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N-Channel MOSFET Small-Signal Darlington Pair based Low-Power Wide-Band Amplifier

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Abstract: N-channel identical MOSFETs based Small-Signal Darlington pair amplifiers under triple transistor topology are simulated at GPDK 180nm, 90nm, and 45nm process technologies in Cadence Virtuoso and Spectre simulation tool. At 180nm technology, amplifier amplifies 1µV-100mV range AC signal with voltage gain (11.656), current gain (105.971), bandwidth (39.4747 GHz), power consumption (25.6708 mW) and THD (0.000031 %). Similarly, at 90nm technology, amplifier is capable of amplifying 1µV-2V ranging AC signal with voltage gain (1.02605), current gain (97.704), bandwidth (91.8932 GHz), power consumption (0.0038 µW) and THD (0.00000034%). However, at 45nm technology, amplifier produces voltage gain (0.0481), current gain (32.2163), higher cut-off frequency (691.367 Hz), power consumption (17.5314 mW) and THD (0.000000004%) with AC signal amplifying range 10 µV-1V. This work also addresses the narrow bandwidth issue of reference amplifier, PNP Sziklai pair amplifier, and poor response issue of proposed amplifier at 45nm technology at higher frequency. Proposed amplifiers are also implemented in Quadrupole topology to test the behavior of the amplifiers. Layout of the proposed amplifiers captures small-area of 2.8858 μm^2 of (1.59 µm X 1.815 µm) dimensions and gives same pre and post layout results. Effect of *w/l* ratio, effect of C_L, effect of different biasing parameters, small-signal AC analysis, temperature dependency and phase variations are among the few studies pursued for the proposed amplifiers. Frequency range suggests their possible application in high pass filter, wireless communication receivers and preamplifiers stages of ECG and seismographs.

Keywords: MOSFET, Cadence, Triple transistor topology, Darlington Pair, Small-signal amplifier, Quadrupole Topology.

1. Introduction

Common-Source MOSFETs amplifiers are generally used to amplify small-signal audio range signals due to its high input impedance, low output impedance, high current gain and voltage gain just greater than unity[1]. However, the Darlington pair, comprises of two identical bipolar transistors, produces high current gain and wide bandwidth at a low frequency, therefore they are being used for high data rate communication system[2]. Darlington pairs are the ideal choice for the applications where high current gain and higher linearity are required[3]. Many small-signal amplifier circuits are examined using Common Source MOSFETs in a Darlington pair configuration[4]. However, the fundamental issue with this setup is that it generates narrow bandwidth signals with high power consumption and high harmonic distortions[5]. Many changes have been suggested over the years to address this issue, such as the insertion of biasing resistances, the use of hybrid active device combinations, or the substitution of Sziklai pairs for Darlington pairs in double- or triple-transistor topologies[6]. In this series, amplifiers with three identical MOSFETs and a few additional resistances and capacitances are proposed, which not only reduces output distortions but also solves the problem of a narrow bandwidth[7-9].

In this paper, three amplifier circuits are proposed using Cadence Virtuoso and Spectre simulation at GPDK 180nm, 90nm, and 45nm process technologies[10-12]. These circuits are based on identical N-channel MOSFETs with a Darlington pair topology, making them suitable for both low- and high-frequency applications[13-14]. Better results in terms of bandwidth, power consumption, and THD are obtained when comparing these amplifiers with the reference amplifier circuit, which is based on commercial Power MOSFETs[15]. Proposed amplifiers are also tested on various scales such as effect of *w/l* ratio, effect of C_L, effect of temperature, Quadrupole topology, Layout and Post-layout simulation, variation of different biasing elements, small-signal AC analysis, Phase variation, determination of performing range for each parameter, and behavior of amplifiers under different conditions. The key merits of the proposed amplifiers are the elimination of the narrow bandwidth issue with reference and PNP Sziklai pair amplifiers as well as the poor response issue with Darlington pair amplifiers at higher frequencies.

2. Experimental Circuit Description

2.1. Circuit Details

Present article comprises the simulation and analysis of N-Channel MOSFET Small-Signal Darlington pair amplifier at GPDK (Generic Process

Device Kits) 180nm, 90nm and 45nm process technologies using Cadence Virtuoso and Spectre Simulation[16].

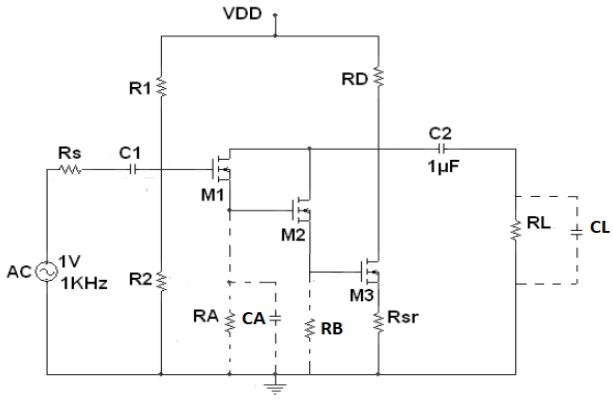

Figure 1. Circuit Design of the Reference and Proposed Amplifiers

Triple transistor topology based Small-Signal Darlington pair amplifier is treated here as "Reference amplifier[15]." Simulated on PSpice simulation software at nearly 2µm technology, this amplifier uses three identical nMOS Power transistors with an additional resistor R_A and capacitor C_A connected between source of first transistor M_1 to ground[17]. However, modified version of the said amplifier is proposed in this paper at 180nm, 90nm and 45nm technologies using Cadence Virtuoso and Spectre simulation and referred here as Proposed Amplifier-1, Proposed Amplifier-2 and Proposed Amplifier-3 respectively.

At 180nm technology, Proposed amplifier-1 includes an extra resistor R_B joined between source of second transistor M_2 to ground along with resistor R_A and capacitor C_A connected between source of first transistor M_1 to ground. Similarly, Proposed amplifier-2 at 90nm technology performs better with two additional resistors R_A and R_B connected between source of M_1 and M_2 to ground respectively. However, at 45nm technology, Proposed amplifier-3 requires only one additional resistor R_B connected between source of M_2 to ground and load capacitor C_L across R_L. Additionally, similar performance is obtained if this resistor is switched to source of M_1 to ground. Basic circuit diagram for the mentioned amplifiers is shown in Figure 1. Position of R_A, C_A, R_B and C_L varies from one amplifier to another; therefore, they are shown by dotted lines.

2.2. Circuital Parameter and Software Details

Table 1 enlists the simulation parameters of nMOS transistors used in Reference and Proposed amplifiers.

Table 1. Simulation Parameters of MOSFETs

MOSFET Model Parameters	Reference Amplifier	Proposed Amplifiers		
		At 180nm Technology	At 90nm Technology	At 45nm Technology
Model Name of M_1, M_2 and M_3 Transistors	IRF150	nmos1	gpdk090_nmos1v	g45n1svt
Cell Name of Each Transistors	---	Nmos	nmos1v	nmos1v
W (Channel Width)	0.3m	2µm	120nm	120nm
L (Channel Length)	2µm	180nm	100nm	45nm
T (Threshold)	---	800nm	120nm	120nm
MW (S/D Metal Width)	---	400nm	120nm	60nm
VTO (Zero-bias threshold voltage)	2.831	0.48	NaN	NaN
GAMMA (Bulk Threshold Parameter)	0	0.666	NaN	NaN
KP (Transconductance)	20.53E-06	0.490	NaN	NaN
PHI (Surface Potential)	0.6	0	0	0
IS (Bulk p-n saturation current)	194E-18	NaN	NaN	NaN
CBD (Bulk-drain zero bias p-n capacitance)	3.229E-09	0	0	0
RD (Drain ohmic resistance)	1.031E-03	0	0	0
RG (Gate ohmic resistance)	13.89	---	---	---
RDS (Drain-source shunt resistance)	444.4E+03	---	---	---
CGSO (Gate-source overlap capacitance)	9.027E-09	370E-12	NaN	NaN
CGDO (Gate-drain overlap capacitance)	1.679E-09	370E-12	NaN	NaN

Table 2. Circuit Components

Circuit Components	Reference Amplifier	Proposed Amplifier-1 at 180nm	Proposed Amplifier-2 at 90nm	Proposed Amplifier-3 at 45nm
R_S (Source Resistance)	250Ω	10Ω	10Ω	10Ω
R_1 (Biasing Resistance)	1.4MΩ	1MΩ	20MΩ	800KΩ
R_2 (Biasing Resistance)	1MΩ	100KΩ	1MΩ	600KΩ
R_D (Drain Resistance)	1KΩ	3KΩ	30KΩ	4KΩ
R_{SR} (Source Biasing Resistance)	100KΩ	10Ω	100KΩ	10Ω
R_A (Additional Biasing Resistance)	300Ω	600Ω	10Ω	Unavailable
R_B (Additional Biasing Resistance)	Unavailable	600Ω	10Ω	10Ω
R_L (Load Resistance)	10KΩ	10KΩ	10KΩ	500Ω
C_1 (Input Capacitor)	10µF	10µF	10µF	10µF
C_2 (Output Capacitor)	1µF	1µF	1µF	100nF
C_A (Additional Capacitors)	100uF	100uF	Unavailable	Unavailable
V_{CC} (Biasing Supply)	+15V	+15V	+15V	+15V

Observations for the Reference as well as Proposed amplifiers are made for 1mV, 1KHz AC input sin wave with +15 Volt DC power supply. Values of the circuit components used in the mentioned amplifiers are listed in Table 2.

3. Results and Discussion

3.1. Performance Parameters

Various performance parameters of the Reference and Proposed amplifiers at 180nm, 90nm and 45nm technologies are recorded in Table 3 at room temperature with the aid of Cadence Virtuoso and Spectre Simulation[18,19]. Figure 2 shows how the voltage gain of the proposed amplifiers varies with respect to frequency for various technologies.

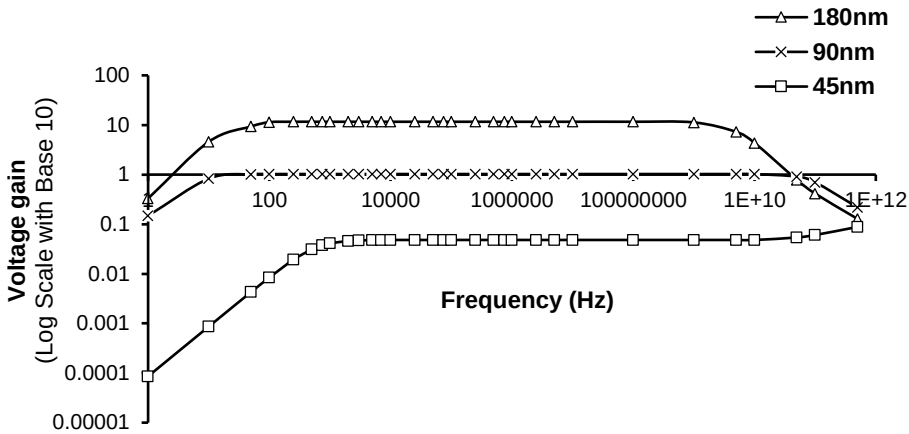

Figure 2. Variation of Voltage gain with frequency

Table 2 suggests that when technology is scaled down to improve the speed of MOSFETs, voltage and current gain of the proposed amplifiers simultaneously reduces[20]. However, bandwidth, power consumption, output referred noise and THD gets improved[21]. This happens because *w/l* ratio of the MOSFETs reduces with reducing technology, therefore transconductance g_m of transistor also decreases as per the relation, $g_m = k' (w / l)(v_{gs} - v_t)$. Since, the voltage gain of the proposed amplifier is directly proportional to g_m hence, voltage gain also decreases[22]. In addition, at 45nm technology, due to the Zener break down at source/substrate junction and Short Channel Effect (channel length becomes equal to the depletion-layer width of source), response curve of voltage gain produces severe distortion[23]. Additionally, in comparison to the reference amplifiers, proposed amplifiers show wider bandwidth, lower power consumption, lower THD and lower output referred noise at 1KHz frequency at the cost of low gain[24].

Table 3 Comparative Table of Performance Parameters

Performance Parameters	**Reference Amplifier**	**Proposed Amplifier at 180nm**	**Proposed Amplifier at 90nm**	**Proposed Amplifier at 45nm**
Amplifier Current Gain A_{IGA}	2652.4	105.971	97.704	32.2163
Upper Cut Off Frequency F_H (for A_{IGA})	37.140 Hz	148.422 MHz	747.693 MHz	5.096 GHz
Lower Cut Off Frequency F_L (for A_{IGA})	26.204 Hz	20.834 Hz	7.2467 Hz	674.715 Hz
Band-Width B_W (for A_{IGA})	10.936 Hz	148.421 MHz	747.692 MHz	5.096 GHz
Amplifier Voltage Gain A_{VGA}	232.12	11.656	1.02605	0.0481
Upper Cut Off Frequency F_H (for A_{VGA})	4.805 KHz	39.4748 GHz	91.8933 GHz	---
Lower Cut Off Frequency F_L (for A_{VGA})	379.32 Hz	20.8392 Hz	7.2385 Hz	691.367 Hz
Band-Width B_W (for A_{VGA})	4.426 KHz	39.4747 GHz	91.8932 GHz	---
Unity Gain Band-Width (for A_{VGA})	854.899 KHz	428.525 GHz	24.7712 GHz	---
Device Voltage Gain A_{VGD}	235.596	11.66	2.3638	0.275
Device Current Gain A_{IGD}	2387.8	575.693 M	11.94 K	540.1466
Input Referred Noise	2.1021 nV/Hz	83.372 $\mu V/\sqrt{Hz}$	164.378 $\mu V/\sqrt{Hz}$	67.9104 $\mu V/\sqrt{Hz}$
Output Referred Noise	480.085 nV/Hz	179.1 $\mu V/\sqrt{Hz}$	45.444 $\mu V/\sqrt{Hz}$	2.7872 $\mu V/\sqrt{Hz}$
Power Gain P_A (in dB-Watt)	57.893	30.917	20.0108	11.9021
Output Voltage Phase Difference θ^O	-168.921	-178.594	-179.576	-147.9787
Phase Margin of Voltage gain θM	---	98.4079	12.7321	Can't be computed
Total Harmonic Distortion THD	0.93%	0.000031%	0.00000034%	0.000000004%
Total Power Consumption, P_W	167 mW	25.6708 mW	0.0038 µW	17.5314 mW
Input Signal Voltage	1 mV at 1KHz	1 mV at 1 KHz	1 mV at 1KHz	1 mV at 1KHz
Permissible Range of Input Signal Voltage	0.1 mV-2 mV	1 µV-100mV	1 µV-2V	10 µV-1V
Slew rate of output voltage	---	0.390 V/µs	0.0413 V/µs	0.875 V/µs
Current across Source Resistance I_{RS}	760.107 nA	11 nA	1.0501 nA	2.991 nA
Current across Load Resistance I_{RL}	24.03 µA	1.1958 µA	103.398 nA	89.4039 nA
Voltage across source resistance V_{RS}	1 mV	1 mV	1 mV	1 mV
Voltage across load resistance V_{RL}	240.28 mV	11.96 mV	1.0343 mV	44.70 µV
Power Spectral Density	---	17.35 nV^2/Hz	1.02 nV^2/Hz	8.7256 pV^2/Hz
Transfer Function	---	11.66 V/V	1.02605 V/V	48.1742 mV/V
Chip Area	---	2.8858 μm^2	---	---

Refer Table 3. Since higher the phase margin (Phase shift at 0dB gain), more stable the amplifier will be[25]. Therefore, proposed amplifier-1 at 180nm technology produces highest phase margin (98.4079°), hence it is more stable than rest of the amplifier's configurations. At 90nm technology, proposed amplifier-2 has widest AC signal amplification range, lowest power consumption and nearly 180° phase shift. Similarly, proposed amplifier-3 at 45 nm technology emerges with highest slew rate (rate of change of output voltage) which must be high in order to produce maximum undistorted output voltage swing[26]. In addition, this configuration also produces lowest output referred noise and lowest THD (approx. tending towards zero) at 1KHz frequency and widest frequency band from 674.715 Hz to 5.096 GHz.

Large difference between current gain A_{IG} and device current gain A_{IGD} of all the proposed amplifiers can be interpreted because the current at resistance R_D suddenly drops to a non-significant value which causes sudden decrease in the overall current gain of the amplifier.

Figure 2 shows that response curve of the proposed amplifier-3 at 45nm technology becomes distorted beyond 100 THz frequency and looks more or less like high-pass filter circuit with cut-off frequency f_H=691.367 Hz which indicates potential application of this amplifier as a "Low-Power High-Pass Filter" in generalized biomedical signal processing circuits[27]. However, poor frequency response nature of this amplifier is further removed by adding load capacitor C_L=1pF across R_L. It is also to be noted that value of the load capacitor must lie within the range $10nF \leq C_L \leq 1fF$. Additionally, proposed amplifier-1 at 180nm technology and Proposed amplifier-2 at 90nm technology produces frequency band from 20.8392 Hz to 39.4747 GHz and 7.2385 Hz to 91.8933 GHz respectively along with low power consumption, low THD and low noise which made them suitable to be used as LNA in Transceiver design in wireless communication system[28]. Main contributions of the proposed amplifier are that they remove the narrow band problem of reference amplifier. Also, proposed amplifier-1 at 180nm, proposed amplifier-2 at 90nm and proposed amplifier-3 at 45nm with C_L successfully eliminate poor frequency response problem of small-signal Darlington pair amplifier at higher frequencies.

3.2. Effect of *w/l* Ratio on the Amplifier Performance

Variation in *w/l* ratio of MOSFETs draws significant impact over the performance parameters, therefore variation of the performance parameters with respect to variation in w/l ratio of respective MOSFETs is studied at 180nm, 90nm and 45nm technologies respectively[29].

A. At 180nm Technology

At 180nm technology, maximum limit of channel width *w* is 50µm and minimum is 400nm with default value of 2µm. Similarly, maximum limit of channel length *l* is infinite whereas minimum limit is 180nm with default value of 180nm. Variation of parameters with *w/l* ratio is listed in Table 4.

Table 4: Variation of parameters at 180nm Technology

***W/L* Ratio**	**Voltage gain**	**Current Gain**	**Bandwidth**	**Power Consumption**
400nm/180nm	4.9975	45.437	92.7044 GHz	21.481 mW
500nm/180nm	5.7867	52.612	88.4591 GHz	21.954 mW
750nm/180nm	7.3563	66.883	82.7117 GHz	22.955 mW
2µm/180nm (Default)	11.656	105.971	39.4747 GHz	25.670 mW
50µm/1µm	14.64	133.039	1.201 GHz	28.200 mW (Distortion)

B. At 90nm Technology

At 90nm technology, channel length varies in the range 100nm ≤ L ≤ 21.68µm with default value of 100nm whereas channel width varies in the range 120nm ≤ W ≤ 30µm with default value of 120nm. Their variation with parameters is listed in Table 5.

Table 5: Variation of parameters at 90nm Technology

***W/L* Ratio**	**Voltage gain**	**Current Gain**	**Bandwidth**	**Power Consumption**
120nm/100nm (Default)	1.0260	97.7041	91.8932 GHz	0.0038 µW
500nm/100nm	2.3959	288.033	41.554 GHz	5.9642 mW
750nm/250nm	3.10698	295.1454	988.103 MHz	3.8595 mW
1µm/500nm	2.4886	232.122	877.926 MHz	2.05 mW
21.68µm/30µm	0.494	14.99	1.2139 GHz	166.52 W

C. At 45nm Technology

At 45nm technology, default value of channel length is 45nm and it can not be greater than 10µm and less than 45nm. Similarly, channel width can not be less than 120nm and greater than 10µm with default value of 120nm. Their variation with parameters is enlisted in Table 6.

Table 6: Variation of parameters at 45nm Technology

***W/L* Ratio**	**Voltage gain**	**Current Gain**	**Bandwidth**	**Power Consumption**
120nm/45nm (Default)	0.040	32.2163	5.096 GHz	17.5314 mW
500nm/100nm	0.036	18.09	1.4755 GHz	25.781 mW
750nm/250nm	0.019	10.57	1.11214 GHz	26.197 mW
1µm/500nm	0.011	4.6151	639.584 MHz	33.3507 mW
10µm/10µm	0.001	1.621	7.5502 MHz	28.92 mW

Refer Table 4, 5 and 6. When *w/l* ratio of MOSFETs at 180nm and 90nm technology is increased; voltage gain, current gain and power consumption simultaneously increases whereas bandwidth reduces. Contrarily, at 45nm technology; voltage gain, current gain and bandwidth reduces with increasing value of *w/l* ratio however power consumption increases.

3.3. Observation under Different Conditions

A. At 180nm Technology

1. When all the extra added resistors R_A, R_B and capacitor C_A are removed from the proposed amplifier-1, voltage gain and current gain both drops to 0.047 and 0.427 respectively. Apart from this, response curve of voltage gain starts behaving as high pass filter with cut-off frequency f_H=5.74255 KHz. Also, power consumption shoots up to 54.693 mW and output voltage and output current transient responses distorted badly. Therefore, it is essential to include these resistors and capacitors to maintain amplifying nature.
2. When R_A and C_A are removed keeping R_B fixed, Voltage and current gain decreases to 0.263 and 2.3997 with distorted output transient waveforms. In addition to it, power consumption also increases to 53.667 mW.
3. Similarly, When R_B is removed keeping R_A and C_A fixed, output voltage transient responses become distorted with voltage and current decreases to 0. 958 and 8.7108 respectively along with 56.44 mW Power Consumption.
4. If C_S=10uF is added across R_{SR}, no effect is reported on parameters.
5. If C_A is removed keeping R_A and R_B fixed, voltage and current gain decreases to 4.3646 and 39.682 respectively with undistorted transient response. Moreover, minor decrement is seen in bandwidth (37.2891 GHz) and power consumption (25.7372 mW).
6. If C_A is added across R_B keeping R_A fixed, voltage gain, current gain and bandwidth decreases to 7.6479, 69.507 and 31.688 GHz respectively. However, power consumption remains unaltered (25.7372 mW).

B. At 90nm Technology

1. When all the added resistors R_A and R_B are removed from the proposed amplifier-2, response curve of current gain is distorted and reaches to 0.692 whereas voltage gain provide poor response at higher frequency and reaches to 0.998 with distorted output current and voltage waveforms. Power consumption also reduces to 1.6043mW. Therefore, it is essential to include these resistors and capacitors.

2. When R_A is removed keeping R_B intact, both voltage as well as current gain curve produces poor frequency responses at higher frequencies. Additionally, current gain reaches to 62.528, voltage gain to 0.656 and power consumption to 4.2183mW.
3. **However, when R_B is removed keeping R_A intact, response of voltage gain becomes poor at higher frequency but both, voltage, and current gain increase to their respective peak values 1.1263 and 107.244 respectively.
4. If C_S=10uF is added across R_{SR}, voltage gain, current gain and bandwidth decreases to 0.993, 94.646 and 79.3294 GHz respectively. However, power consumption becomes higher (3.8621 mW).

C. At 45nm Technology

1. When the added resistor R_B is removed from proposed amplifier-3, voltage gain becomes very much small and reaches to 0.004 whereas current gain decreased to 2.9151 and shows poor response at higher frequency. However, power consumption becomes very high and reaches to 12.83 W.
2. If the position of resistor R_B is changed i.e., if it is connected between M_1 to ground, same result is obtained. This is the unique result which is not generally found in small-signal amplifiers.
3. If both R_A and R_B are added, current and voltage gain decreased to 0.329 and 0.015 respectively whereas power consumption increases to 25.47 mW.
4. If C_S=10uF is added across R_{SR}, all parameters remain unchanged.

3.4. Performing Range of the Circuit Components

At 180nm technology (Proposed amplifier-1), minimum value of amplifier voltage gain A_{VGA} is received at R_S=960KΩ ($A_{VG\text{-}MIN}$=1.0083) and maximum value at R_S=1Ω ($A_{VG\text{-}MAX}$=11.6566) with meaningful amplification in $1\Omega \leq R_S \leq 1.3M\Omega$ range. Similarly, values of R_1 and R_2 must be kept within the range $500K\Omega \leq R_1 \leq 1M\Omega$ and $20K\Omega \leq R_2 \leq 600K\Omega$ respectively. Moreover, maximum, and minimum limit of R_D in order to produce amplification is 50KΩ and 38KΩ respectively. Also, value of R_A and R_B must be kept less than or equal to 20KΩ. In addition, value of the C_A must lie within the range $100mF \leq C_A \leq 10uF$ because when the C_A exceeds 10uF, voltage response curve produces poor response at higher frequency.

At 90nm technology (Proposed amplifier-2), value of R_S must be kept less than or equal to 20KΩ. Also, lower limit for R_1 is 50MΩ, however there is no maximum limit for R_1 because after a critical value, voltage gain remains constant at increasing value of R_1 whereas boundary condition for R_2 is $200K\Omega \leq R_2 \leq 1M\Omega$. Moreover, meaningful amplification corresponds to R_D

is received within the range $20K\Omega \leq R_D \leq 100K\Omega$. In addition, value of added resistances R_A and R_B must be less than or equal to $2K\Omega$ to receive amplification.

At 45nm technology (Proposed amplifier-3), during observation an important finding is received that when the value of the source resistor R_S exceeds $50K\Omega$, poor response problem of this particular amplifier at higher frequency is removed without adding any load capacitor across R_L[30]. Current gain reaches its minimum value 1.00473 at $R_1=500K\Omega$ and maximum value 44.7162 at $R_1=1M\Omega$. Similarly, R_2 provides purposeful amplification in the $400K\Omega \leq R_2 \leq 1M\Omega$ range. In the same way, current gain reaches its minimum value 8.9139 at $R_D=1K\Omega$ and maximum value 30.5528 at $R_D=10K\Omega$. However, boundary limit for R_B should be $R_B \leq 1K\Omega$ in order to receive distortion-less response.

3.5. Effect of Load Capacitor C_L

Effect of load capacitor C_L on the performance of the amplifiers has also been studied at 180nm, 90nm and 45nm technologies respectively using Cadence Virtuoso and Spectre simulation[21,22].

At 180nm technology, proposed amplifier-1 produces meaningful amplification for the range $10\mu F \leq C_L \leq 1nF$. For example, at $C_L=1nF$, performance parameters for proposed amplifier-1 are - $A_{VG}=11.656$ $B_W=136.144$ MHz $A_{IG}=105.9708$ and Total Power Consumption=25.6707mW. Similarly, at $C_L=10\mu F$, performance parameters are as follows- $A_{VG}=1.01836$ $B_W=180.614$ Hz $A_{IG}=9.4388$ Total Power Consumption=25.6315 mW.

Similarly, at 90nm technology, proposed amplifier-2 works effectively with the load capacitor C_L in the range $10\mu F \leq C_L \leq 1pF$. At $C_L=1pF$, performance parameters for the proposed amplifier-2 are - $A_{VG}=0.048$ $B_W=432.171$ MHz $A_{IG}=32.2162$ Total Power Consumption=17.531 mW. Similarly, at $C_L=10\mu F$, parameters for the proposed amplifier-2 obtained are as follows - $A_{VG}=0.002$ $B_W=95.112$ Hz $A_{IG}=1.72783$ Total Power Consumption=17.5314 mW.

It is noteworthy that the proposed amplifier-3 at 45nm technology produces poor response at higher frequency ($\geq$100THz)[23,24]. Therefore, inclusion of load capacitor as a basic circuital element in this amplifier removes the poor response problem at higher frequency[25]. Performing range of C_L for producing distortion-less response is $10nF \leq C_L \leq 1fF$. Parameters at $C_L=1fF$ is - $A_{VG}=01.02605$ $B_W=22.5698$ GHz $A_{IG}=97.704$ Total Power Consumption=3.8620 mW. Similarly, at $C_L=10nF$, parameters are - $A_{VG}=1.02138$ $B_W=1.98$ Hz $A_{IG}=97.2593$ Total Power Consumption=3.8620

mW. In addition, poor response problem of this amplifier at higher frequency is also resolved when C_L reaches 100fF.

Observations indicate that at higher values of load capacitors within the specified range, proposed amplifiers produce narrow bandwidth i.e., 180.614 Hz for proposed amplifier-1, 95.112 Hz for proposed amplifier-2 and 95.112 Hz for proposed amplifier-3. Therefore, these amplifiers may be used for the amplification of δ, θ, α, β and γ waves released by human brain if used at preamplifier stage in EEG signal acquisition circuit. These amplifiers may also be used as pre-amplifier in seismograph for the amplification of seismic waves emerged during earthquake[26,27].

3.6. Variational Effect of Amplifier with Different Parameters

3.6.1. Effect of DC Supply Voltage on Total Power Consumption

Variation of total power consumption of all the amplifiers with respect to DC supply voltage is shown in Figure 3[28,29].

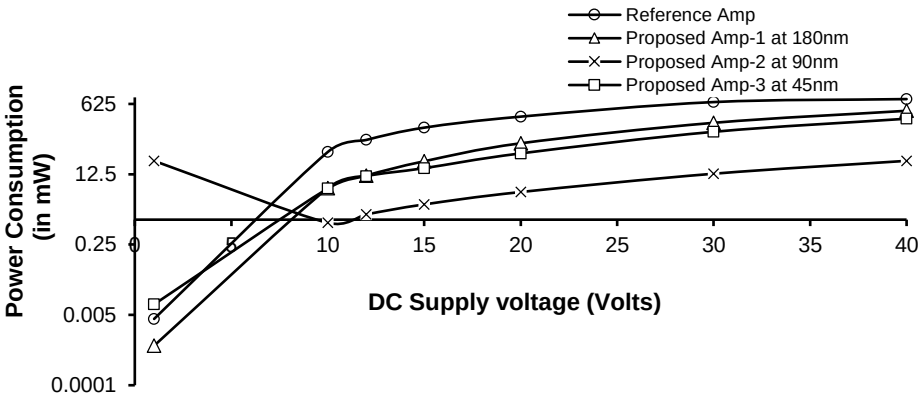

Figure 3. Variation of Power Consumption with DC Supply Voltage

It has been seen that power consumption is directly proportional to the DC supply voltage. For the reference amplifier, power consumption decreases with increasing DC supply voltage up to 10V[15]. However, beyond this value, power consumption starts increasing with increasing DC supply voltage. Contrarily, for the proposed amplifiers, power consumption increases with increasing DC supply voltage.

3.6.2. Variation of Voltage Gain with Added Resistance

Variation of the voltage gain of all the amplifiers with respect to added resistance is also shown in Figure 4[30].

Voltage Gain of the reference amplifier and proposed amplifier-3 at 45nm technology decreases with increasing value of added resistance R_A[15].

However, for proposed amplifier-1 at 180nm technology, voltage gain initially increases with increasing value of R_A up to R_A/R_B=1KΩ. But beyond this value, it starts decreasing with increasing R_A and produces distortion in the response curve. Similarly, for the proposed amplifier-2 at 90nm technology, voltage gain remains constant up to R_A=5KΩ and thereafter starts decreasing with increasing R_A. In addition, when $R_A \geq 5K\Omega$, severe distortion is received in the voltage gain response curve.

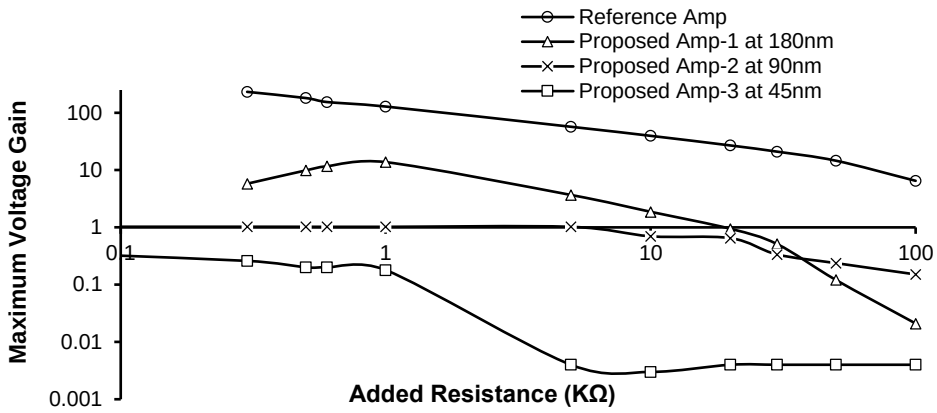

Figure 4. Variation of Voltage Gain with Added Resistance

Boundary condition for added resistance R_A in the proposed amplifier-1 is R_A, $R_B \leq 20K\Omega$, proposed amplifier-2 is R_A, $R_B \leq 2K\Omega$ and proposed amplifier-3 is $R_B \leq 3K\Omega$.

3.6.3. Variation of Voltage Gain with Drain Resistance

Variation of voltage gain with respect to drain resistance is depicted in Figure 5[10,11].

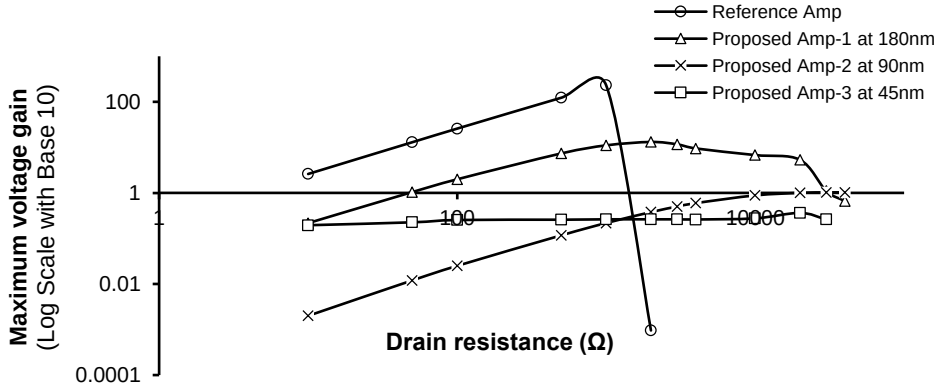

Figure 5. Variation of Voltage Gain with Added Resistance

Reference and Proposed amplifier-1 at 180nm technology increases with increasing value of R_D up to R_D=1KΩ and decreases thereafter[15]. Similarly, voltage gain of the proposed amplifier-2 at 90nm technology, increases with increasing R_D. However, voltage gain of the proposed amplifier-3 at 45nm technology, almost remains constant with increasing value of R_D.
Performing range of proposed amplifier-1 corresponds to R_D is 38KΩ ≤ R_D ≤ 500KΩ, proposed amplifier-2 is 20KΩ ≤ R_D ≤ 100KΩ and proposed amplifier-3 is 1KΩ ≤ R_D ≤ 10KΩ.

3.6.4. Variation of Voltage Gain with DC Supply Voltage

Variation of voltage gain with respect to DC Supply Voltage is depicted in Figure 6[12,13].

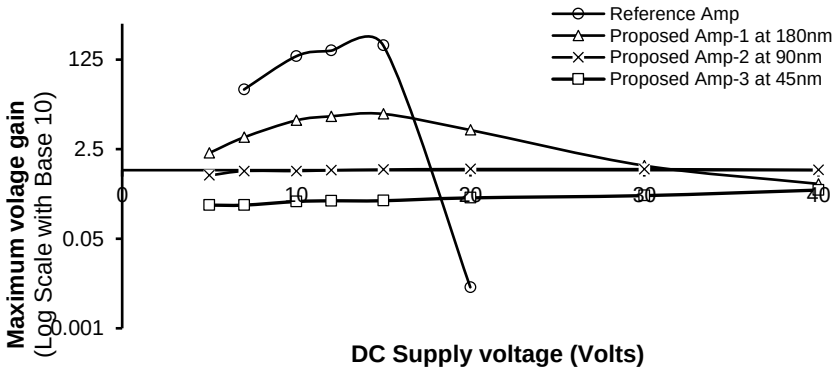

Figure 6. Variation of Voltage Gain with DC Supply Voltage

Reference amplifier switches-ON at V_{CC}=7 Volts and its voltage gain rises non-linearly with increasing value of supply voltage up to V_{CC}=15 Volts and decreases sharply above this value[15]. Similarly, proposed amplifier-1 at 180nm technology switches-ON at V_{CC}=2 Volts and its voltage gain increases non-linearly upto V_{CC}=15 Volt and decreases thereafter. However, proposed amplifier-2 at 90nm technology switches-ON at V_{CC}=15 Volt and remains almost constant with increasing value of V_{CC}. Similarly, Voltage gain of the proposed amplifier-3 at 45nm technology, increases with a slow pace with increasing DC supply voltage.

3.6.5. Variation of Voltage Gain with Source Resistance

Variation of Voltage gain as a function of source resistance has also been studied for all the amplifiers under consideration[14]. It is found that Voltage gain of the proposed amplifiers almost remain constant with respect to variation in R_{SR}. However, voltage gain of the reference amplifier initially increases up to R_{SR}=5KΩ and acquire saturation trend at higher values of R_{SR}[15].

3.7. Effect of Temperature Dependency

Impact of temperature on the performance of the proposed amplifiers have also been studied and respective observation corresponds to proposed amplifier-1, proposed amplifier-2 and proposed amplifier-3 have been recorded in Table 7, Table 8 and Table 9 respectively[16].

Table 7. Variation of parameters of Proposed amplifier-1 with Temperature

Temperature (°C)	Proposed Amplifier-1 at 180nm			
	Voltage Gain	Current Gain	Bandwidth	Power Consumption
-20	13.7544	125.054	39.5432 GHz	25.1131 mW
0	12.7663	116.07	39.4551 GHz	25.3720 mW
10	12.329	112.098	39.414 GHz	25.4887 mW
27	11.656	105.971	39.3747 GHz	25.6708 mW
50	10.852	98.6656	39.2014 GHz	25.8920 mW
80	9.9408	90.3816	39.0423 GHz	26.1535 mW

Table 8. Variation of parameters of Proposed amplifier-2 with Temperature

Temperature (°C)	Proposed Amplifier-2 at 90nm			
	Voltage Gain	Current Gain	Bandwidth	Power Consumption
-20	1.14315	108.8566	95.754 GHz	4.1232 mW
0	1.09555	104.3231	94.067 GHz	4.0103 mW
10	1.07047	101.9345	93.129 GHz	3.9549 mW
27	1.02605	97.704	91.8932 GHz	3.8000 mW
50	0.962	91.6167	90.0549 GHz	3.7382 mW
80	0.876	83.4149	88.291 GHz	3.5824 mW

Table 9. Variation of parameters of Proposed amplifier-3 with Temperature

Temperature (°C)	Proposed Amplifier-3 at 45nm			
	Voltage Gain	Current Gain	Bandwidth	Power Consumption
-20	0.026	17.7848	5.12114 GHz	23.8528 mW
0	0.025	17.9364	5.1412 GHz	23.8489 mW
10	0.020	18.8935	5.1737 GHz	23.7453 mW
27	0.048	32.6163	5.1960 GHz	17.5314 mW
50	0.045	30.282	5.2145 GHz	16.9186 mW
80	0.042	27.768	5.2741 GHz	16.0865 mW

Refer Table 7 and 8. Voltage gain, current gain, and bandwidth of proposed amplifier-1 at 180nm technology and Proposed amplifier-2 at 90nm technology decreases as the temperature range increases. However, power consumption of the proposed amplifier-1 increases whereas for proposed

amplifier-2, it decreases with increasing temperature. This happens because drain-source resistance of the composite unit rises with temperature which in turn reduces the voltage gain, current gain and bandwidth[15].

Table 9 shows that when the temperature of proposed amplifier-3 at 45nm technology increases, bandwidth simultaneously increases whereas power consumption decreases. However, current gain initially increases up to 27°C and starts decreasing beyond this value and voltage gain varies in zig-zag manner. Output coupling capacitor C_2 at proposed amplifier-3 bears low capacitance (of the order of 100nF value) which causes reduction in effective circuit capacitance which consequently widens the bandwidth with increasing temperature[17].

3.8. Phase Variation

Phase shift of output current of proposed amplifier-1 at 180nm, proposed amplifier-2 at 90nm and proposed amplifier-3 at 45nm technology with respect to input current is listed in Table 10[18,19].

Table 10. Phase Variation with Frequency

Frequency	**Phase Difference of Output Current with input current in θ°**		
	Proposed Amplifier-1 at 180nm	**Proposed Amplifier-2 at 90nm**	**Proposed Amplifier-3 at 45nm**
1 Hz	-77.4827	-97.3488	-87.37745
10 Hz	-99.7668	-144.3467	-90.73734
100 Hz	-165.7883	-176.0042	-100.1353
1 KHz	-178.7123	-179.5814	-149.7504
10 KHz	-179.8589	-179.9594	-176.7059
100 KHz	-179.9857	-179.9959	-179.6623
1 MHz	-180.0003	-180.0003	-179.9667
10 MHz	-180.0153	-180.0069	-179.9975
100 MHz	-180.1539	-180.0698	-180.008

Refer Table 10. At operating frequency, proposed amplifier-1 produces highest phase difference (-179.5814°) than all other amplifier configurations. Also, proposed amplifier-1 and Proposed amplifier-2 produces 180° output phase shift in the frequency range 1 MHz-100 MHz. Similarly, proposed amplifier-3 produces phase shift at 100 MHz frequency. However, reference amplifier produces 180° output current phase shift at around 1.38 KHz frequency[15].

3.9. Mathematical Analysis

Small-signal AC equivalent circuit for the Proposed Amplifier-1 at 180nm is shown in Figure 7[20,21].

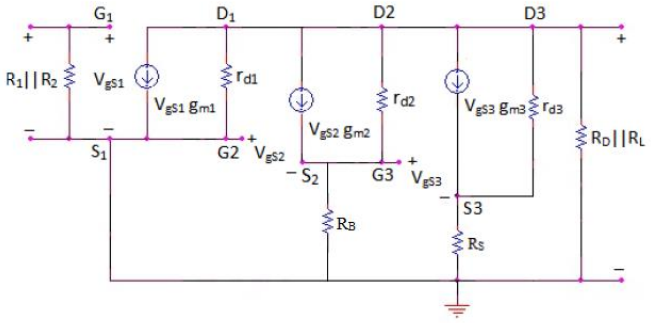

Figure 7. Small Signal AC Circuit of Proposed amplifier-1

Input impedance of this circuit ($R_1 \| R_2$) is 90909.09 Ω which is much higher than its output impedance ($R_L \| R_D$) which is 2307.692 Ω. Similar to the reference amplifier circuit, nMOS transistor M_2 are also treated here as absent as output current of transistor M_2 is zero[15]. Therefore, equation for the AC voltage gain is given by

$$A_{VG} = \frac{-g_{m1}\left(1 + g_{m3}R_S - \frac{R_S}{r_{d3}}\right)}{\frac{1}{R_o} + \frac{1}{R_o}\left(g_{m3}R_S - \frac{R_S}{r_{d3}}\right)}$$

where $R_o = R_L \| R_D$.

3.10. Layout and Post-layout Simulation

Figure 8 depicts the Layout of the proposed amplifier-1 at 180nm technology is also designed using Layout XL Editor tool[12].

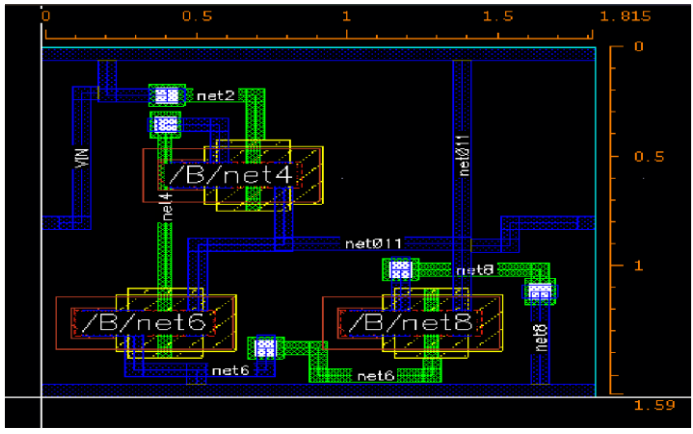

Figure 8. Layout of Proposed amplifier-1 at 180nm Technology

Area of the layout is around 2.8858 μm^2 (1.59 μm X 1.815 μm). All the MOSFETs are taken as 'Integrated' rather than 'Detached' because in each

MOSFETs, substrate is directly connected to the source[23]. Horizontal rail is applied at GND and V_{DD} pins to avoid overlapping whereas IN and OUT pins are fixed at left and right corners respectively[24]. Dimension of M_1 is 0.68µm X 0.955µm whereas for M_2 and M_3, it is 0.39µm X 0.28µm and 1.275µm X 0.28µm respectively. DRC and LVS run shows no errors and give almost same pre and post layout simulation results under acceptable percentage variation range[15]. As compared to pre-layout simulation, post-layout simulation result of current gain (100.004), voltage gain (9.330) and power consumption (20.133mW) shows 5.79391%, 22.1672% and 24.1805% respectively. Graphical representation of pre and post layout simulation results is shown in Figure 9.

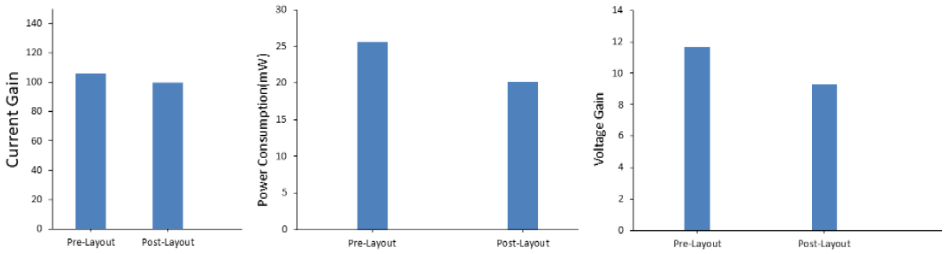

Figure 9. Pre and Post Layout Simulation Results

3.11. Proposed Amplifier's Performance under Quadrupole Arrangement

Rather than just the triple transistor topology, proposed amplifiers are also tested with the Quadrupole transistor topology (having four identical MOSFETs) to see how it behaves in different circuit structures. This topology was first proposed by *Hassen* in 2013[14].

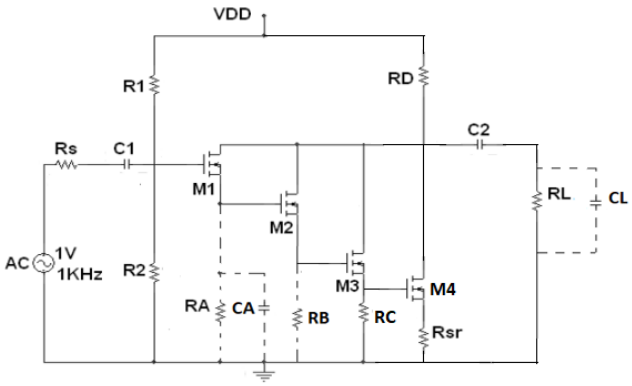

Figure 10. Proposed amplifier under Quadrupole Topology

In this circuit, we have inserted another identical nMOS transistor M_4 whose gate is joined with the source of M_3[17,18]. It also employs one added resistor R_C=10Ω connected between source of M_3 to ground with distinct value of the load resistor R_L=1KΩ. Figure 10 shows the proposed amplifier under Quadrupole topology. Comparison of parameters at 180nm technology in Triple Transistor topology and proposed Quadrupole topology is listed in Table 11.

Table 11. Comparative Table of Parameters under Quadrupole Topology

Parameters	**Under Quadrupole Topology at 180nm**	**Under Triple Transistor at 180nm**
Voltage gain	6.9708	11.656
Low Cut-off Frequency	23.667 Hz	20.8392 Hz
High Cut-off Frequency	44.7954 GHz	39.4748 GHz
Bandwidth	44.7953 GHz	39.4747 GHz
Current gain	633.775	105.971
Power Consumption	22.0444 mW	25.6708 mW
Output Noise	10.466 μV/$\sqrt{Hz}$	179.1 μV/$\sqrt{Hz}$
Input Noise	1.50197 μV/$\sqrt{Hz}$	83.372 μV/$\sqrt{Hz}$
THD	0.000011%	0.000031%

Table 11 clearly shows that proposed amplifier under quadrupole topology produces high current gain, wide bandwidth, low THD, low output and input noise, low THD, and low power consumption than triple transistor topology at the expense of low voltage gain[19]. Therefore, this topology could serve as a basis for further investigation on the proposed amplifiers to give them more prominence.

4. Conclusion

Triple Transistor Toplogy based Small-signal Darlington pair amplifier circuits with identical NMOS transistors available at GPDK 180nm, 90nm and 45nm process technologies are analyzed in this paper using Cadence Virtuoso and Spectre simulation tool. Narrow bandwidth problem of reference amplifier and PNP Sziklai pair amplifier are removed by the proposed amplifiers alongwith consuming low power and producing low THD.

It is also found that as the technology is scaled down, number of passive components in the circuit decreases simultaneously which causes reduction in voltage and current gain and increment in bandwidth. Poor frequency response problem of the amplifier at 45nm technology is removed by adding C_L across R_L and exceeding the value of R_S beyond 50KΩ. Inclusion of C_L in

the proposed amplifiers within the specified range helps them to operate in low frequency range (<100Hz) for the amplification of seismic waves and alpha, beta, gamma and delta waves released by human brain.

Proposed amplifiers are also implemented in Quadrupole topology which shows improved results than triple transistor topology. With small-area of 2.8858 μm^2 having dimensions of 1.59 µm and 1.815 µm, proposed amplifiers show same pre and post layout simulation results which validate the amplifiers in 180nm technology. Analysis of the proposed amplifiers suggest their use in high pass filter and as LNA in transceiver design in wireless communication system.

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