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Darlington Pair based Small-Signal Amplifier under Triple-Transistor Topology

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Abstract: Small-Signal Darlington pair amplifiers with MOS-BJT-MOS hybrid unit under triple transistor topology are demonstrated using PSpice and GPDK 180nm technology in Cadence Virtuoso and Spectre tool. The first circuit under Cadence tool produces moderate voltage gain (5.156), high current gain (2165.6), wide bandwidth (15.8866 GHz), high power gain (40.4789 dB-Watt), low power consumption (556.556 mW) with low THD (11.85E-6 %) and could be used in Radar, TV and wireless communication receivers where as the second circuit with PSpice user defined model generates high voltage gain (933.235), very high current gain (44207), wide bandwidth (16.275 MHz), high power gain (76.1548 dB-Watt), low power consumption (71.6mW) and low THD (1.18%), thus it may be used in AM radio broadcast, marine and aeronautical communications. Respective amplifiers are compared with previously announced commercial transistor-based circuit which shows very promising result in terms of voltage gain, current gain, and power consumption. Proposed amplifiers are also physically verified in the Cadence using virtuoso layout editor tool which shows that it covers a small area of 80.0124 μm^2 with a dimension of 8.97µm x 8. 92µm. Small-signal AC analysis, different configurations of the proposed amplifier, variation of the voltage gain with respect to different circuit components are amongst the few studies attempted in the present paper.

Keywords: PSpice, Cadence, Triple transistor topology, Darlington Pair, Small-signal amplifier.

1. Introduction

Darlington pair has successfully demonstrated its importance in amplifying small-signals[1]. The Darlington transistor (often known as a

double-emitter follower, super α circuit, super β transistor and β multiplier) comprises of two identical bipolar transistors coupled with each other so that the second transistor amplifies the current produced by the first transistor[2]. This configuration has a diverse range of applications that extends from power amplifier circuits to small-signal amplifier circuits[3]. Although it has better current gain characteristics, its response degrades more quickly than that of a single transistor at higher frequencies[4].

Therefore, Darlington pair amplifiers have undergone numerous revisions in an effort to solve this issue over the past few decades[5]. The employment of different active devices or hybrid active device combinations in a triple or double Darlington topology, as well as the addition of certain additional biasing resistances in the appropriate amplifier circuits, are a few of the more well-liked attempts[6]. However, a new field of study is currently being conducted on the use of the dissimilar active devices in the Darlington pair topology[7].

This paper proposes circuit models of small-signal Darlington pair amplifiers with hybrid combination of MOS-BJT-MOS using PSpice and Cadence Virtuoso tool at GPDK 180nm technology. Proposed amplifiers successfully eliminate the poor frequency response problem of Darlington pair at higher frequency[8]. These amplifiers are also compared with the Darlington pair small-signal amplifier circuit announced by Srivastava et al[9]. In terms of current gain, bandwidth and output referred noise, proposed amplifiers outperform all the previous circuits, available in the literature, on Darlington pair small-signal amplifiers used in wireless communication network. Detailed physical analysis of the related parameters of the proposed amplifiers are also performed in this paper.

2. Research Method

Present study consists of design and analysis of the triple transistor topology-based Darlington pair small-signal amplifier using PSpice and Cadence virtuoso and Spectre tool at GPDK 180nm technology. Small-signal Darlington pair amplifier with commercial transistors proposed by Srivastava et al. is considered here as Reference Amplifier[9] (Figure 1). However, its modified versions with transistors available in Cadence Virtuoso and Spectre simulation tool at GPDK 180nm technology and PSpice user defined transistors are reported here as Proposed Amplifier-1 and Proposed Amplifier-2 respectively (obeying similar circuit design of Figure 1).

All the amplifiers, discussed here, consist of two identical nMOS transistors and one BJT connected in cascading way with BJT in the middle under Darlington pair configuration. The nMOS transistor M_1 and npn

transistor Q_1 forms first Darlington pair while the npn transistor Q_1 and nMOS transistor M_2 collectively represents second Darlington pair. Apart from this, two additional resistors R_{AD} and R_A connected between source of M_1 to ground and emitter of Q_1 to ground respectively, help in minimizing distortion and retaining amplification property.

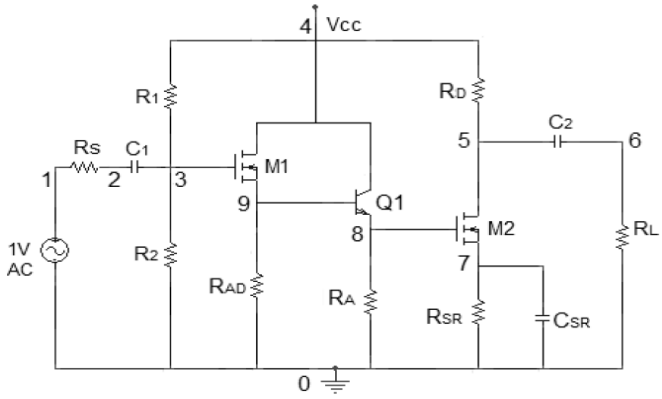

Figure 1. Circuit Design of the Reference and Proposed Amplifier

Proposed amplifier-1, in Cadence virtuoso tool, uses lateral type of BJTs and nMOS transistors, extracted from Analog (Spectre) foundry under bipolar.net and nmos.net file available at GPDK 180nm technology respectively whereas Proposed Amplifier-2 employs user defined transistors available in PSpice tool.

Table 1 Simulation Parameters of BJTs

BJT Model Parameters	Q2N2222 (NPN BJT)	QN (NPN BJT)	Npn (NPN BJT)
IS (p-n saturation current)	14.34E-15	1E-15	3.26E-12
BF (Ideal maximum forward beta)	255.9	100	100
BR (Ideal maximum reverse beta)	6.092	50	6
RC (Collector ohmic resistance)	1	0.1	1
TF (Ideal forward transit time)	411.1E-12	200E-12	25E-12
TR (Ideal reverse transit time)	46.9E-09	5E-09	200E-12
CN (Base-Collector leakage emission coefficient)	2.42	2.42	2

Table-1 and Table-2 show the simulation parameters of bipolar junction transistors and nMOS transistors available in PSpice and Cadence virtuoso tool at GPDK 180nm technology respectively. Transistor Q2N2222 and nMOS transistor IRF150 shows the commercial version of the amplifier, transistor QN and nMOS transistor NMOD resperents user defined models of the amplifier whereas transistor npn and nMOS transistor nmos1 represents the schematic of the proposed amplifier in Cadence Virtuoso and Spectre simulation at GPDK 180nm technology.

Table 2 Simulation Parameters of MOSFETs

MOSFET Model Parameters	IRF150 (N-Channel MOSFET)	NMOD (N-Channel MOSFET)	nmos1 (N-Channel MOSFET)
W (Channel Width)	0.3	100E-06	5e-6
L (Channel Length)	2E-06	100E-06	5e-6
VTO (Zero-bias threshold voltage)	2.831	3	0.48
GAMMA (Bulk Threshold Parameter)	0	0	0.666
KP (Transconductance)	20.53E-06	14.54	0.490
PHI (Surface Potential)	0.6	0.6	0
IS (Bulk p-n saturation current)	194E-18	10E-15	NaN
CBD (Bulk-drain zero bias p-n capacitance)	3.229E-09	5E-12	0
CBS (Bulk-Source zero bias p-n capacitance)	---	2E-12	0
RB (Bulk ohmic resistance)	---	---	---
RD (Drain ohmic resistance)	1.031E-03	5	0
RG (Gate ohmic resistance)	13.89	---	---
RDS (Drain-source shunt resistance)	444.4E+03	1E+06	---
CGSO (Gate-source overlap capacitance)	9.027E-09	1E-12	370E-12
CGDO (Gate-drain overlap capacitance)	1.679E-09	1E-12	370E-12
CGBO (Gate-bulk overlap capacitance)	0	1E-12	NaN

Amplifiers are biased with +18V DC supply voltage and 1mV, 1KHz AC input sin wave using potential divider network with circuit parameters as described in Table 3.

Table 3 Component Details of the amplifiers

Circuit Components	Reference Amplifier	Proposed Amplifier-1	Proposed Amplifier-2
M1 (N-Channel MOSFET)	IRF150	NMOD	nmos1
Q1 (NPN BJT)	Q2N2222	QN	npn
M2 (N-Channel MOSFET)	IRF150	NMODN	nmos1
R_S (Source Resistance)	500Ω	10Ω	10Ω
R_1 (Biasing Resistance)	1.3MΩ	900KΩ	700KΩ
R_2 (Biasing Resistance)	1MΩ	1MΩ	300KΩ
R_D/R_{CD} (Drain Resistance)	5KΩ	5KΩ	1KΩ
R_{SR} (Source Biasing Resistance)	1KΩ	1KΩ	900Ω
R_A (Additional Biasing Resistance)	10KΩ	10KΩ	300Ω
R_{AD} (Additional Biasing Resistance)	10KΩ	10KΩ	300Ω
R_L (Load Resistance)	10KΩ	10KΩ	500Ω
C_1, C_2 (Coupling Capacitors)	1μF	10μF	10Ω
C_A/C_{SR} (Bypass Capacitors)	100μF	1mF	1mF
V_{CC} (Biasing Supply)	+18VDC	+18VDC	+18VDC
V_{IN} (AC Signal)	1mV-10mV(1KHz)	1mV-10nV(1KHz)	100uV-100mV

3. Results and Discussion

3.1. Performance Parameters

Table 4 comprises the simulation data of various performance parameters of the proposed and reference amplifier with the aid of PSpice and Cadence

Virtuoso and Spectre simulation at GPDK 180nm technology[10,11]. However, Figure 2 depicts the variation of current gain with respect to frequency.
Table-4 and Figure-2 suggests that proposed amplifier-2 with PSpice user defined models produces higher voltage gain, higher current gain, wider bandwidth, low output referred noise, and wider AC signal amplification range than reference amplifier at the expense of high THD and high-power consumption[12].On the other hand, despite the fact that proposed amplifier-1 simulated at GPDK 180nm technology in Cadence Virtuoso tool doesn't produce higher voltage and current gain than reference amplifier, it might be utilized inpre-amplifier stages in wireless communication receiver due to its widest bandwidth and lowest harmonic distortion[13]. Low voltage and current gain nature of this amplifier is generally due to the small-channel length MOSFETs available at GPDK 180nm technology[14].

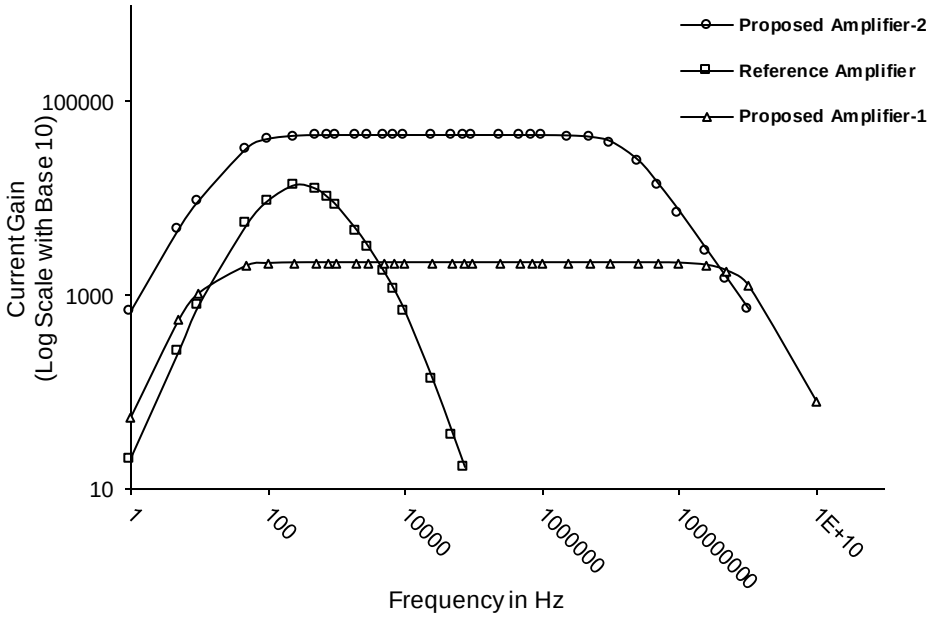

Figure 2. Variation of Current gain with frequency

Figure 2 suggests that Proposed amplifier-1 performs in SHF (Super High Frequency) range, thus it could be used in Radar, TV and wireless communication receivers whereas Proposed Amplifier-2 works in HF (High frequency range) which indicates its use in AM radio broadcast, Marine and aeronautical communications[15]. Additionally, both the proposed amplifiers successfully eliminate poor frequency response problem of small-signal Darlington pair amplifier at higher frequencies[16].

Table 4 Comparative Table of Performance Parameters

Performance Parameters	Reference Amplifier	Proposed Amplifier-1	Proposed Amplifier-2
Amplifier Voltage Gain A_{VGA}	311.593	5.156	933.235
Upper Cut Off Frequency F_H (for A_{VGA})	9.817 KHz	15.8867 GHz	16.276 MHz
Lower Cut Off Frequency F_L (for A_{VGA})	151.056 Hz	17.9569 Hz	45.066 Hz
Band-Width B_W (for A_{VGA})	9.665 KHz	15.8866 GHz	16.275 MHz
Unity Gain Band-Width (for A_{VGA})	1.1402 MHz	87.2967 GHz	1.986 GHz
Amplifier Current Gain A_{IGA}	13971	2165.6	44207
Upper Cut Off Frequency F_H (for A_{IGA})	814.382 KHz	702.077 MHz	16.225 MHz
Lower Cut Off Frequency F_L (for A_{IGA})	104.498 Hz	-1.5311 KHz	45.295 Hz
Band-Width B_W (for A_{IGA})	814.381 KHz	702.066 MHz	16.224 MHz
Device Voltage Gain A_{VGD}	312.037	8.7563	933.254
Device Current Gain A_{IGD}	326.336 K	578.97 G	10.014 T
Input Referred Noise	3.1238 nV/Hz	18.99 nV^2/Hz	825.101 pV/Hz
Output Referred Noise	972.249 nV/Hz	19.9 nV^2/Hz	769.238 nV/Hz
Power Gain P_A (in dB-Watt)	66.3881	40.4789	76.1548
Output Voltage Phase Difference θ^O	-176.826	-178.813	-177.376
Phase Margin θ_M of Voltage gain	---	102.23	---
Total Harmonic Distortion THD	0.8%	11.85E-6 %	1.18%
Total Power Consumption, P_W	43.9 mW	556.556 mW	71.6 mW
Input Signal Voltage	1mV at 1KHz	1 mV at 1KHz	1mV at 1KHz
Permissible Range of Input Signal Voltage	1-10 mV	100uV-100mV	1mV-10nV
Slew rate of output voltage	---	0.1639 V/us	---
Current across Source Resistance I_{RS}	3.7491 nA	9.094 uA	2.1091 nA
Current across Load Resistance I_{RL}	31.494 uA	4.7621 nA	94.149 uA
Voltage across source resistance V_{RS}	1 mV	1 mV	1 mV
Voltage across load resistance V_{RL}	314.923 mV	4.55 mV	941.337 mV
Power Spectral Density	----	19.99 nV^2/Hz	----
Transfer Function	----	5.156 V/V	---
Chip Area		80.0124 μm^2	

3.2. Layout

Virtuoso Layout Editor tool is used here for layout capture[16]. Figure 3 shows the layout of the proposed amplifier covers a small area of 80.0124 μm^2 having 8.97 µm x 8.92 µm dimensions.

Both the proposed amplifiers show no error during DRC and LVS run which validates the proposed design. It is also found that the proposed amplifier produces 2% variation in voltage gain as compared to pre-layout simulation data thus verifying the proposed designs in 180nm technology.

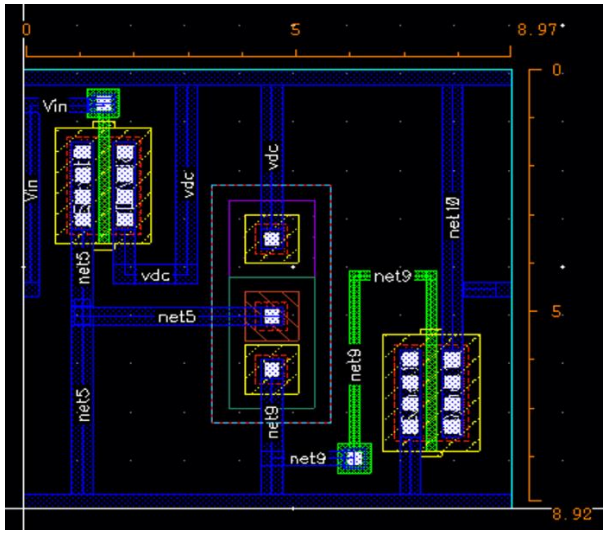

Figure 3. Layout of the proposed amplifier

3.3. Small-Signal AC Analysis

Small-signal AC equivalent circuit of the proposed amplifier is depicted in Figure-4[13,17,20].

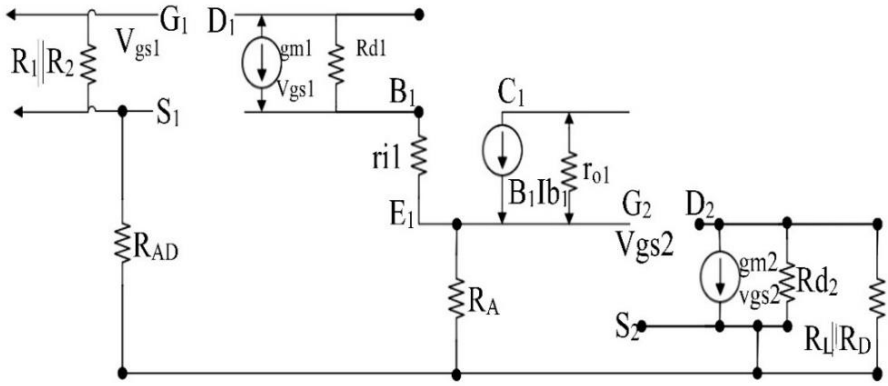

Figure 4. AC Equivalent circuit of the Proposed amplifier

Analysis of Figure 4 shows that the input impedance of the proposed amplifier is very high ($R_1 \parallel R_2$= 2100Ω) in comparison to the output impedance ($R_L \parallel R_D = 333.33\Omega$).

Using KCL, following equations can be framed for Figure 4,

(1) $$\mathrm{V}d1 = -i_{d1} \times (R_{d1}) = -g_{m1} v_{gs1} (R_{d1}) \qquad [i_{d1} = g_{m1} v_{gs1}]$$

(2) $$i_{b1} + \beta_1 i_{b1} + i_{o1} = 0$$

(3) $$V_o = i_o (R_L \parallel R_D)$$

(4) $$V_{in} = i_{b1}(R_1 \parallel R_2)$$

(5) $$\mathrm{V}d2 = -i_{d2} \times (R_{d2}) = -g_{m2} v_{gs2}(R_{d2}) \qquad [i_{d2} = g_{m2} v_{gs2}]$$

Based on the above equations, expression for the current gain might takes the following form-

$$A_{IG} = \frac{i_o}{i_{b1}}$$

$$A_{IG} = \frac{-g_{m1} g_{m2} \beta r_o}{R_O R_{AD} \left(\frac{1}{1 - \frac{r_\pi}{R_B}} \right)}$$

3.4. Effect of Additional Resistor R_A and R_{AD}

Variation of maximum voltage gain with added resistances R_A and R_{AD} for both the amplifiers is also studied[18,19].

For the reference amplifier, maximum voltage gain increases only a bit at increasing values of R_A and R_{AD} and finally acquires a state of saturation beyond 50KΩ[9].Similarly, for proposed amplifier-2, maximum voltage gain increases with increasing value of R_A and R_{AD}. However, for proposed amplifier-1, increasing value of R_A and R_{AD} causes voltage gain to decrease simultaneously and vice-versa. In addition, some interesting findings are also quoted -

1. If R_{AD} is removed keeping R_A intact in Proposed amplifier-1, voltage gain, current gain, bandwidth, and power consumption decreases to 4.639, 1.9505K, 874.773 MHz (F_H=874.774 MHz and F_L=18.402 Hz) and 324.081mW respectively.
2. If R_A is removed, keeping R_{AD} intact in Proposed amplifier-1, voltage gain decreases to 3.3517, current gain to 1.4078K and Power consumption to 347.317mW whereas bandwidth increases to 17.470 GHz (F_H=17.471 GHz and F_L=18.977 Hz).
3. If R_A and R_{AD} both are removed from Proposed amplifier-1, response curve of voltage and current gain reaches to zero with distorted output. However, bandwidth reaches to 52.42b THz (F_H=55.42 THz and F_L=3.0503 THz).

3.5. Effect of Additional Resistor R_{SR}

Variation of maximum voltage gain with Source resistance R_{SR} is shown in Figure-5[20]. For the reference amplifier, at increasing values of R_{SR}, A_{VG} found its maximum value at R_{SR}=0.5KΩ, thereafter, decreases almost

exponentially to reach below unity at 50KΩ[9]. Similarly, for proposed amplifier-2, A_{VG} found its maximum value at R_{SR}=1KΩ, thereafter, decreases almost exponentially. However, for proposed amplifier-1, A_{VG} increases with increasing value of R_{SR} and reaches its maximum value at R_{SR}=1KΩ and thereafter start decreasing exponentially and reaches below unity at R_{SR}=25KΩ. This is due to the source degeneration property of common source MOSFET amplifier which forces voltage gain to fall almost exponentially with increasing R_{SR}[9].

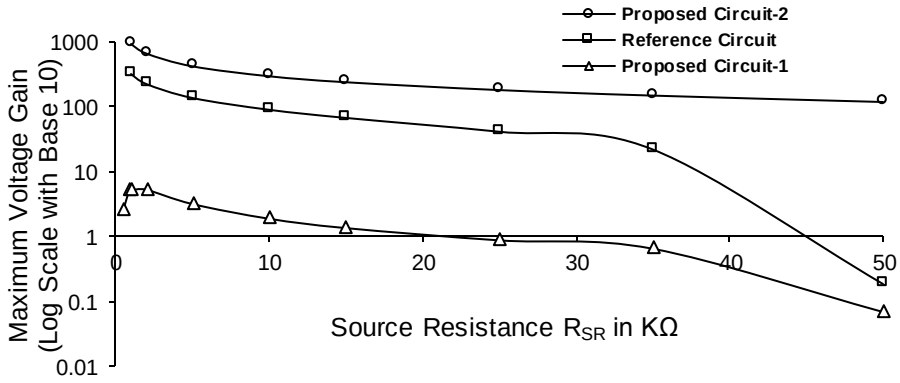

Figure 5. Variation of Voltage Gain with R_{SR}

3.6. Effect of Drain Resistance R_D

Variation of maximum voltage gain with drain resistance R_D is depicted in Figure-6[19,20] .

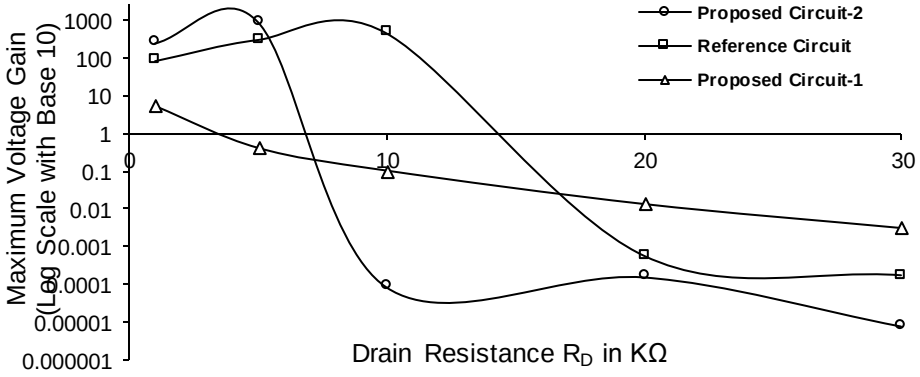

Figure 6. Variation of Voltage Gain with R_D

For the reference amplifier, the voltage gain increases with R_D and attains a maximum at R_D=10KΩ, thereafter, the circuit starts producing a distorted output[9]. Similarly, for proposed amplifier-2, voltage gain reaches to its maximum value at R_D=5KΩ and reaches below unity beyond this value. However, for proposed amplifier-1, maximum value of voltage gain is attained at R_D=1KΩ, and reaches below unity at R_D=10KΩ. Thereafter, it starts to give distorted output.

3.7. Effect of Load resistor R_L

Variation of maximum voltage gain with load resistance is also studied[10-13,20]. For all the amplifiers under discussion, maximum voltage gain A_{VG} rises to R_L=100KΩ and acquire a saturation tendency at higher values of R_L. This rising and saturation of the voltage gain with R_L is found in accordance with the usual behavior of small signal amplifiers[9].

3.8. Effect of DC Supply Voltage

Variation of maximum voltage gain A_{VG} with DC supply voltage V_{CC} is depicted in Figure 7[16-20].

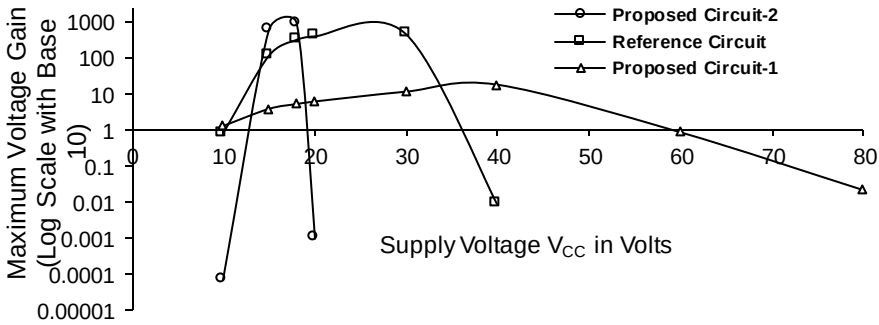

Figure 7. Variation of Voltage Gain with V_{CC}

For the reference amplifier, A_{VG} increases non-linearly from 10V to 30Vof V_{CC}, thereafter, drops to a lowest point at V_{CC}=40V.The range for the reproduction of the output at different V_{CC} for reference amplifier is 15-30V[9]. Similarly, for proposed amplifier-2, A_{VG} increases non-linearly and reaches to its maximum value at V_{CC}=18V, and thereafter goes below unity at higher V_{CC}. This usually happens because when V_{CC} reaches beyond 18V, amplifier receives better flow of electron from source to drain, thus drain absorbs more electrons. Consequently, channel pinched-off and causes voltage gain to decrease. Contrarily, for proposed amplifier-1, A_{VG} increases non-linearly with increasing value of V_{CC} and drops to zero at V_{CC} = 60V. However, above V_{CC} = 60V, this amplifier shows distortion in the output.

3.9. Effect of Temperature

Variation of maximum voltage gain with respect to temperature ranging between -20°C to 80°C is summarized in Table-5[15-18].

For the reference amplifier, voltage gain, current gain and bandwidth decreases with rising temperature[9]. Similarly, for proposed amplifier-1 and proposed amplifier-2, all these three parameters drop as temperature rises. However, power consumption for the proposed amplifiers increases with increase in temperature. Reduced parameters typically results because the mobility of majority carriers decreases at higher temperature which lowers the drain current of nMOS transistor M_2, lowering voltage and current[9].

Table 5 Variation of Performance Parameters with Temperature

Temperature (°C)	Proposed Amplifier-1				Proposed Amplifier-2			
	A_{VG}	A_{IG}	Bandwidth	Power Consumption	A_{VG}	A_{IG}	Bandwidth	Power Consumption
-20	6.1375	2577.9	17.88 GHz	555.530 mW	1029	47113	16.22 MHz	69.9 mW
0	5.6768	2384.4	16.86 GHz	555.983 mW	984.59	44020	17.01 MHz	69.9 mW
10	5.4712	2298.4	16.37 GHz	556.201 mW	964.53	44164	17.21 MHz	70.0 mW
27	5.516	2165.6	15.60 GHz	556.556 mW	933.235	44207	16.27 MHz	71.6 mW
50	4.7808	2008.0	14.92 GHz	557.010 mW	895.67	43212	15.10 MHz	74.9 mW
80	4.3612	1831.8	14.16 GHz	557.551 mW	853.41	43116	15.00 MHz	75.5 mW

3.10. Phase Variation

Table 6 depicts the variation of phase with respect to frequency for all the amplifiers under consideration[12,14,20].

Table 6 Phase Difference with respect to frequency

Frequency	Phase Difference of Output Current in $\theta°$		
	Reference Amplifier	Proposed Amplifier-1	ProposedAmplifier-2
1 Hz	-47.916	-65.31	-51.698
10 Hz	-54.513	-72.21	-97.203
100 Hz	-118.255	-80.4	-155.256
1 KHz	-176.826	-178.813	-177.376
10 KHz	-226.313	-222.311	-182.772
100 KHz	-277.011	-265.221	-180.326
1 MHz	-380.022	-498.331	-183.514
10 MHz	-458.03	-500.221	-211.219
100 MHz	-492.012	-511.284	-261.056

For all the amplifiers, phase reversal output is received in their respective outputs. This generally happens because CE and CS configuration of BJT and MOSFETs produce 180° phase shift in their respective output waveforms. Additionally, for all the discussed amplifiers, Phase difference reduces as the frequency range increases[9].

3.11. Configurations other than Proposed amplifiers

During simulation, four different structures have also been realized such as Case-1, Case-2, Case-3, and Case-4 whose performance parameters are listed in Table 7[16-20]. These cases are listed below-

1. When Q_1 and Q_2 of the amplifier are taken as NPN transistor and M_3 as NMOS transistor (i.e., BJT-BJT-MOS), the circuit configuration of Figure 1 designates Case- 1 amplifier design[16].
2. If Q_1 and Q_3 are taken as NPN transistor and NMOS transistor as M_2 (i.e., BJT-MOS-BJT), the circuit configuration of Figure 1 represents Case-2 amplifier design[17].
3. When in Figure 1 circuit design, Q_1 is taken as NPN transistor and M_2 and M_3 as NMOS transistor (i.e., BJT-MOS-MOS), the circuit configuration of figure 1 represents Case-3 amplifier design[18].
4. When Q_3 is taken as NPN transistor and M_1, M_2 as NMOS transistor (i.e., MOS-MOS-BJT), the circuit configuration of Figure 1 represents Case-4 amplifier design[19].

All the four cases are simulated with commercial transistors, modelled transistors, and transistors available at GPDK 180nm technology in PSpice and Cadence virtuoso and Spectre simulation tool respectively. The application ranges of all the amplifiers indicated in Tables 7(A), 7(B), 7(C), and 7(D) appear to be the same as those stated in Table 4 due to their similar performance parameters. However, Commercial model-based version of these amplifiers suffers in bandwidth reduction[20].

Component and simulation parameters for these Cases are same as discussed in Table 1, Table 2, and Table 3. However, Case-3 amplifier in GPDK 180nm technology in Cadence tool uses R_S=500Ω, R_1=600KΩ, R_2=900KΩ, R_{AD}=R_A=300Ω, R_D=6KΩ, R_L=500Ω, R_{SR}=900Ω, C_{SR}=100uF and C_1=C_2=10uF. Similarly, Case-4 amplifier in GPDK 180nm technology in Cadence tool employs R_S=500Ω, R_1=900KΩ, R_2=600KΩ, R_{AD}=R_A=100Ω, R_D=5KΩ, R_L=1KΩ, R_{SR}=1KΩ, C_{SR}=100uF and C_1=C_2=10uF.

Table 7 (A) Performance parameters of the Case-1

Performance Parameters	With Cadence Virtuoso tool at GPDK180nm	With PSpice User Defined Model	With PSpice Commercial Model
A_{IG}	2244.4	66034	36615
F_L	1.5867 Hz	433.454 Hz	214.393 Hz
F_H	1.36076 GHz	24.335 MHz	38.435 KHz
B_W	1.3606 GHz	24.334 MHz	38.335 KHz
A_{VG}	2.9835	221.288	110.272
Power Gain in dB-Watt	38.2582	71.647	66.0612
Power Consumption	879.825 mW	65.9 mW	1.06 W
THD	45.11E-f%	1.79%	0.98%

Table 7 (B) Performance parameters of the Case-2

Performance Parameters	With Cadence Virtuoso tool at GPDK180nm	With PSpice User Defined Model	With PSpice Commercial Model
A_{IG}	7843.7	21203	8292.1
F_L	5.54 KHz	139.584 Hz	58.544 Hz
F_H	1.0856 MHz	26.361 MHz	65.687 KHz
B_W	1.0855 MHz	26.360 MHz	65.686 KHz
A_{VG}	206.892	70.847	195.759
Power Gain in dB-Watt	62.1026	61.7671	62.1038
Power Consumption	706.370 mW	61.6 mW	466 mW
THD	43.21E-6%	0.90%	0.90%

Table 7 (C) Performance parameters of the Case-3

Performance Parameters	With Cadence Virtuoso tool at GPDK180nm	With PSpice User Defined Model	With PSpice Commercial Model
A_{IG}	191.918	54332	31344
F_L	11.694 Hz	420.924 Hz	199.720 Hz
F_H	8.87406 MHz	28.747 MHz	36.119 KHz
B_W	8.97405 MHz	28.746 MHz	36.018 KHz
A_{VG}	5.5166	216.192	105.976
Power Gain in dB-Watt	30.2478	70.6989	65.2136
Power Consumption	98.300 mW	1.03 W	159 mW
THD	9.9164E-06%	1.79%	1.70%

Table 7 (D) Performance parameters of the Case-4

Performance Parameters	With Cadence Virtuoso tool at GPDK180nm	With PSpice User Defined Model	With PSpice Commercial Model
AIG	11000	40024	32921
FL	171.494 Hz	165.482 Hz	120.741 Hz
FH	63.6294 MHz	897.687 MHz	959.824 Hz
BW	63.6293 MHz	897.686 MHz	839.18 Hz
AVG	30.523	84.405	87.965
Power Gain in dB-Watt	65.2136	65.2868	64.6178
Power Consumption	1.5974 W	182 mW	720 mW
THD	34.887E-6%	0.95%	0.95%

4. Conclusion

The proposed study centered around the modeling and analysis of two circuit models of small-signal Darlington pair amplifier under MOS-BJT-MOS hybrid unit. First circuit uses model available at GPDK 180nm technology in Cadence whereas the other one employs PSpice user defined model. Their comparison with commercial model shows very promising result in terms of current gain, voltage gain, bandwidth, and power consumption.

With high current gain, medium voltage gains and nearly 180° phase shift in output current suggests that the proposed amplifiers behave more or less like typical CE- amplifier. At 1 KHz of the operating frequency, proposed amplifier-1 produces lowest output referred noise with lowest THD and phase reversal output close to 180° than proposed amplifier-2. As compared to pre-layout simulation data, the proposed amplifier provides only 2% variation in voltage gain, which validates the proposed designs in 180nm technology. Four different cases based on the possible combination of MOS-BJT-MOS has also been proposed and it is found that the commercial version-based amplifiers produce narrow bandwidth with low voltage and current gain.

It is also found that different circuit parameters for the proposed amplifiers are required for modelling in both simulation tools since MOSFETs available in PSpice and GPDK 180nm technology in Cadence Virtuoso tool have different aspect ratios. Additionally, proposed amplifiers successfully remove poor frequency response problem of small-signal Darlington pair at higher frequency. Frequency band of the proposed amplifiers operating in SHF- and HF-range points their potential application in Radar, TV, wireless communication receivers, AM radio broadcast, Marine and aeronautical communications.

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