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Small-Signal Sziklai pair based Tuned Amplifiers with Low Power High Gain

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Abstract: New triple transistor topology based two circuit models of PNP driven Sziklai pair small-signal amplifiers have been proposed and analyzed in this paper. First circuit uses matched BJTs while second circuit employs lateral type of unmatched BJTs available at Generic Process Design Kits (GPDK) 180nm technology in Cadence virtuoso Spectre simulation. Transistor Q1 and Q2 in proposed circuit constitute PNP Sziklai whereas transistor Q2 and Q3 collectively represents NPN Sziklai. Matched BJT based circuit works on very low AC input signal 0.1nV-3mV and generates moderate amplifier current gain (9.568), higher amplifier voltage gain (234.899), wider bandwidth (3.8126 MHz), higher power gain (33.517 dB-Watt) with low THD (0.778%) while second circuit based on BJTs available at GPDK 180nm technology, amplifies AC signal ranging between 10 nV-1 µV with higher voltage gain (252.106), moderate current gain (7.6838), wider bandwidth (212.597 MHz), low power consumption (119.596 mW) and low THD (25.3027 u%) than earlier reported commercial BJTs based Sziklai pair small-signal amplifier under triple transistor topology. Excellent thermal stability of the proposed amplifier combined with low level input and output noises over operational temperature range -30ºC ≤T≤+50ºC exemplifies predominant features of these amplifiers. Present article includes detailed physical analysis of related parameters.The layout of the proposed amplifier takes up a small area of 1157.6124 µm2 (12.68µm×12.43 µm) giving same pre and post layout simulation results.

Keywords: PSpice Simulation, Sziklai pair, Complementary Darlington Pair, Small-signal amplifier, current gain factor.

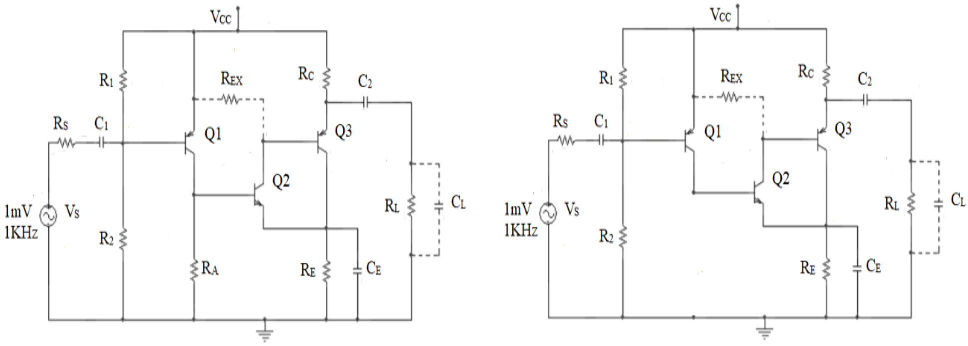
1. Introduction

Sziklai pair is a combination of two transistors of opposite polarity with collector of the first BJT drives the base of the second and emitter of both BJT is kept common[1,2]. Sziklai pair and Darlington pair has almost identical range of current gain, input resistance, output resistance and voltage gain but Sziklai pair is preferred over Darlington pair due its better response at higher frequencies, better linearity due to low quiescent current, better thermal stability due to lower heat dissipation, half base turn-ON voltage (V_{BE}=0.65 Volts)[3-5]. However, its current gain factor ($\beta_{Q1}\beta_{Q2}+\beta_{Q1}$) is generally reduced due to in-built negative feedback[6].

Darlington pairs are widely used to design small-signal and power amplifiers as it delivers high gain at low frequency[7-9] whereas Sziklai pairs are used in the output stages of push-pull power amplifiers[10-12]. However, use of Sziklai pair in the small-signal amplifier and other linear electronic circuits are under the stage of development. Over the past one decade, many small-signal amplifiers with different combinations of BJTs, JFETs, and MOSFETs under Sziklai pair have been configured[13-15].

Present study mainly based upon the comparison between the various performance parameters of PNP Sziklai small-signal amplifier with commercial BJT under triple transistor topology and its modified version with user defined PSpice model of matched BJTs and lateral type of unmatched BJT available at GPDK 180nm technology in Cadence. Both the proposed amplifier delivers higher current and voltage gain, wider bandwidth with low THD, low power consumption and works on very low range of AC input voltage than earlier announced small-signal amplifier of Shukla et. al.[16].For the variation of $R_S$within the range 3KΩ-7KΩ, proposed amplifier may be used in preamplifier stages of PPG (Photoplethysmography) signal amplification circuit to monitor the shape of the blood pressure signal[17-18]. Tuning capability of these amplifiers also make them suitable to be used in radio and TV receiver stages. Layout and post-layout simulation of the proposed amplifier has also been performed on the cadence virtuoso tool. It is found that layout design of the proposed amplifier takes up a small area of 1157.6124 μm^2 (12.68μm×12.43 μm). In addition, performance parameters of proposed amplifier are nearly same before and after layout, thus it verifies the proposed designs in 180nm technology.

2. Circuit Description and Research Method



(A) (B)

Figure 1. Circuit Design of the Proposed Amplifier under (A) PSpice tool (B) Cadence virtuoso tool

Present work includes a comparative discussion among the various performance parameters of two PNP-driven Sziklai pair small-signal amplifier under triple transistor topology. Commercial transistors based PNP Sziklai small-signal amplifier is referred here as 'Reference amplifier' (Figure 1A)[16]while its modified versions with PSpice user defined model of BJTs (Figure 1A) and with Cadence virtuoso model of lateral type BJTs, extracted from are extracted from Analog (Spectre) foundry under bipolar.net file available at GPDK 180nm technology (Figure 1B), are attempted in this paper and represented as 'Proposed amplifiers'. Object properties of both lateral types BJTs are- Emitter width=0.6 nm, Area=0.36 nm^2 and Multiplier=1. Transistor Q_1 and Q_2 constitute PNP Sziklai whereas transistor Q_2 and Q_3 collectively represents NPN Sziklai. Resistance R_{EX} and capacitor C_L is used here as an optional biasing component as R_{EX} is employed to observe circuit behavior under different conditions whereas C_L is used to measure tuning capability of the proposed amplifier. Proposed circuits have been simulated using PSpice tool and Cadence virtuoso tool at 180nm technology.

It is important to note that the reference and proposed amplifiers under PSpice tool (Figure 1A) require additional biasing resistance R_A to maintain its amplification property while the same amplifier under Cadence virtuoso tool (Figure 1B) does not require any additional biasing resistance in its circuital configuration to produce meaningful results[19].

Reference amplifier (Figure 1A) uses Q2N2907A BJT (β=231.7) as PNP transistor & Q2N2222 BJT (β=255.9) as NPN transistor in PNP Sziklai configuration and Q2N2222 BJT as NPN transistor & Q2N2907A BJT as PNP transistor in NPN Sziklai configuration under Sziklai pair triple transistor topology with biasing components such as RS=200Ω, R1=47KΩ, R2=100KΩ, RC=10KΩ, RE=2KΩ, RA=500Ω RL=10KΩ C1=10µF C2=10µF CE=0.001µF and VCC= +18 Volt. Proposed amplifier under PSpice tool (Figure 1A) uses QP BJT (β=240) as PNP transistor & QN BJT (β=240) as NPN transistor in PNP Sziklai configuration and QN BJT as NPN transistor & QP BJT as PNP transistor in NPN Sziklai configuration under Sziklai pair triple transistor topology with biasing components such as RS=1Ω, R1=47KΩ, R2=100KΩ, RC=12KΩ, RE=5KΩ, RA=500Ω RL=10KΩ C1=10µF C2=10µF CE=0.1nF and VCC= +18 Volt. Similarly, this amplifier under Cadence virtuoso tool (Figure 1B) uses pnp BJT (β=35) as PNP transistor &pnp BJT (β=100) as NPN transistor in PNP Sziklai configuration and npn BJT as NPN transistor &pnp BJT as PNP transistor in NPN Sziklai configuration under Sziklai pair triple transistor topology with biasing components such as RS=1Ω, R1=500KΩ, R2=100KΩ, RC=100KΩ, RE=2KΩ, RL=5KΩ C1=100µF C2=100nF CE=0.1fF and VCC= +18 Volt. BJT model parameters used in PSpice and Cadence virtuoso tool have been listed in Table 1.

Table 1: Simulation Parameters

BJT Model Parameters	**Reference Amplifier under PSpice tool**			**Proposed Amplifier under PSpice tool**			**Proposed Amplifier under Cadence virtuoso tool at GPDK 180nm Technology**		
	Q2N2907A (PNP BJT)	***Q2N2222 (NPN BJT)***	***Q2N2907A (PNP BJT)***	***QP (PNP BJT)***	***QN (NPN BJT)***	***QP (PNP BJT)***	***pnp (PNP BJT)***	***npn (NPN BJT)***	***pnp (PNP BJT)***
IS (p-n saturation current)	650.60 E-18	14.34E-15	650.60E-18	200.00E-12	200.00 E-12	200.00 E-12	3.28E -16	3.26E -16	3.28E -16
BF (Ideal maximum forward beta)	231.7	255.9	231.7	115	115	115	35	100	35
BR (Ideal maximum reverse beta)	3.563	6.092	3.563	10	10	10	6	6	6
RC (Collector ohmic resistance)	0.715	1	0.715	0.1	0.1	0.1	1	1	1
TF (Ideal forward transit time)	603.7E-12	411.10E-12	603.7E-12	200.00E-12	200.00 E-12	200.00 E-12	25E-12	25E-12	25E-12
TR (Ideal reverse transit time)	111.3E-09	46.91E-09	111.3E-09	5.00E -09	5.00E-09	5.00E-09	200E -12	200E -12	200E -12
CN (Base-Collector leakage emission coefficient)	2.2	2.42	2.2	2.2	2.42		2	2	2

3. Circuit Description and Research Method

3.1. Performance Parameters

Comparative variations between the performance parameters of reference and proposed amplifiers are recorded at room temperature 27°C and listed in Table 2. Frequency response curve of voltage gain and current gain of all the amplifiers are depicted in Figure 2 and Figure 3 which shows that the proposed amplifiers have a better response of voltage and current gain than reference amplifier[16].

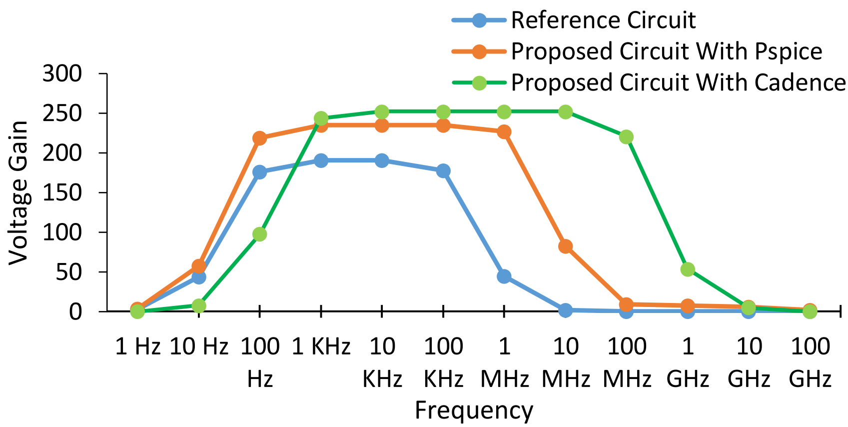


Figure 2. Frequency response curve of voltage gain of the Amplifiers under discussion

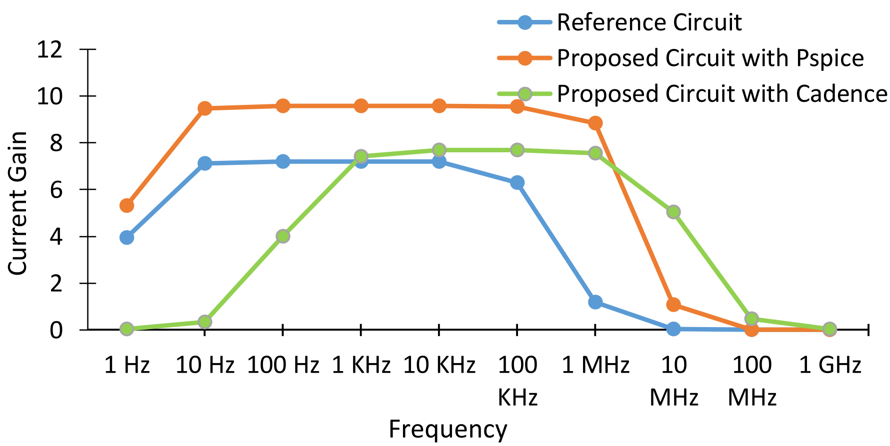


Figure 3. Frequency response curve of Current gain of the Amplifiers under discussion

Table 2 clearly indicates that the use of Cadence virtuoso model of lateral type BJTs available at GPDK 180nm technology[19]and exclusion of additional biasing resistance R_A in the circuit design of proposed amplifier causes meaningful improvement in the performance parameters which in-turns generates high gain, wide bandwidth, low noise, low THD and consumes very low power as compared to all the other amplifiers under discussion. In addition to it, each amplifier uses 1 V 1KHz AC input signal however, the observations are carried out for 1 mV 1KHz AC input signal. It is found that reference and proposed amplifier under PSpice tool can amplify and produce undistorted output for 1µV-10mV and 0.1nV-3mV range of AC input signal at 1KHz frequency respectively[20]. Similarly, proposed amplifier under Cadence tool produces fair response for 10 nV-1 uV range of AC input signal.

Table 2: Comparative Table of Performance Parameters

Performance Parameters	**Proposed Amplifier**		**Reference Amplifier**
	Under Cadence tool	***Under PSpice tool***	***Under PSpice tool***
Amplifier Voltage Gain A_{VGA}	252.106	234.899	190.950
Upper Cut Off Frequency F_H (for A_{VGA})	212.598 MHz	3.8127 MHz	250.872 KHz
Lower Cut Off Frequency F_L (for A_{VGA})	234.786 Hz	39.076 Hz	41.915 Hz
Band-Width B_W (for A_{VGA})	212.597 MHz	3.8126 MHz	250.871 KHz
Unity Gain Band-Width (for A_{VGA})	23.5332 GHz	782.621 MHz	531.89 MHz
Amplifier Current Gain A_{IGA}	7.6838	9.568	7.2086
Upper Cut Off Frequency F_H (for A_{IGA})	5.64905 MHz	2.2554 MHz	181.792 KHz
Lower Cut Off Frequency F_L (for A_{IGA})	230.958 Hz	1.5100 Hz	1.5390 Hz
Band-Width B_W (for A_{IGA})	5.6488 MHz	2.2551 MHz	180.223 KHz
Device Voltage Gain A_{VGD}	356.459 (Distortion)	245.993	418.237
Device Current Gain A_{IGD}	7.6977	17.694	14.433
Power Gain P_A (in dB-Watt)	32.871	33.517	21.22
Output Voltage Phase Difference θ^O	-165.27	-177.692	-177.742
Phase Margin θ_M of Voltage gain	158.914	----	----
Total Harmonic Distortion THD	25.3027 u%	0.778%	0.817%
Total Power Consumption, P_W	119.596 mW	661 mW	642 mW
Input Signal Voltage	1mV at 1KHz	1mV at 1kHz	1mV at 1KHz
Permissible Range of Input Signal Voltage	10 nV-1 uV	0.1 nV-3mV	1µV-10mV
Slew rate of output voltage	1.3 V/ms	----	----
Current across Source Resistance I_{RS}	6.339 uA	2.3880 uA	2.5758 uA
Current across Load Resistance I_{RL}	39.22 uA	24.085 uA	19.719 uA
Voltage across source resistance V_{RS}	1 mV	0.9991 mV	1 mV
Voltage across load resistance V_{RL}	196.099 mV	250.809 mV	197.205
Power Spectral Density	3.1742 fV^2/Hz	----	----
Input Noise	223.95 pV/sqrt (Hz)	231.760 pV/sqrt (Hz)	2.3942 nV/sqrt (Hz)
Output Noise	55.059 nV/ sqrt (Hz)	54.399 nV/sqrt (Hz)	456.843 nV/sqrt (Hz)
Transfer Function	252.105 V/V	----	----
Chip Area	12.62 µm × 12.74 µm	----	----

It is also to be mentioned that load capacitor C_L has been excluded from the amplifiers during observations. It therefore becomes necessary to study and analyze the behavior of these amplifiers in the presence of C_L. When C_L= 10µF is added in the proposed amplifier under PSpice tool, voltage gain drops to 114.113, current gain drops to 9.1810, bandwidth becomes narrow to 73.387 Hz (F_H = 89.220 Hz and F_L = 15.833 Hz) and THD climbs to 4.055%. Similarly, when reference amplifier is added with C_L= 10µF, voltage gain clips down to 99.443, current gain decreased to 6.9703, bandwidth becomes much narrow i.e., 88.537 Hz (F_H = 106.873 Hz and F_L = 18.336 Hz) and higher level of distortion is received with THD = 3.68%[16]. Similarly, when the load capacitor C_L=10µF is added in the proposed amplifier under cadence virtuoso tool (Figure 1B), voltage gain drops to 3.4438 (with F_L=11.3209 Hz F_H=850.222 Hz, B_W=838.9011 Hz), current gain to 0.106 (with F_L=3.4382 Hz F_H=856.55 Hz, B_W=853.1114 Hz), total power consumption remains constant at 119.857 mW and THD goes down to 18.589 u%. Thus, load capacitor C_L should not be added in the circuit design of the proposed and reference amplifier during analysis.

3.2 Effect of Additional Biasing Resistance R_A

Proposed amplifier under PSpice tool (Figure 1A) require additional biasing resistance R_A while under Cadence virtuoso tool, no additional biasing resistance R_A is needed in the design of proposed amplifier (Figure 1B). Table 3 shows the status of performance parameters when R_A is removed from Figure 1A and when R_A=500Ω is added between collector of Q_1 to ground in Figure 1B simultaneously[21].

It is apparent from the Table 3 that when R_A is removed from the proposed amplifier (Figure 1A) under PSpice tool, voltage gain reduced to 1.7493, current gain dips below unity, THD increased to 2.87%. However, bandwidth expands to 21.206 MHz. It has also been found that response curve of voltage gain becomes unstable at the frequencies greater than 100 MHz on the removal of R_A from the proposed amplifier. This happens because, increase in R_A causes simultaneous increase in base voltage to NPN transistor Q_2. This causes current through R_E to increase and current through R_L and therefore A_{VG} to reduce[22]. It therefore becomes essential to include R_A in the circuit design of the proposed amplifier. It is very important to note that proposed amplifier becomes un-realistic for range 1Ω <R_A< 180 Ω because within this range, difference between AC Voltage gain and transient Voltage gain becomes much higher. For example, At R_A = 150 Ω, AC voltage gain comes out to be 11788 whereas in transient analysis, it is equal to 92.17. Besides this, output voltage waveform becomes distorted at R_A = 1 Ω with THD as high as 507.6%. Therefore, range of R_A to produce meaningful voltage amplification is $R_A > 180\Omega$.

Similarly, when $R_A=500\Omega$ is added between collector of Q_1 to ground under Cadence virtuoso tool, voltage gain goes down to 117.493, current gain to 1.22, THD increased to 32.87u%, total power consumption increased to 121.876 mW and bandwidth becomes much narrow to 200.11KHz (with F_H=201.002 KHz and F_L=1.32 Hz). Therefore, inclusion of R_A in the circuit design of the proposed amplifier (Figure 1B) should not be a good choice, but if gain is not an issue, then this amplifier could be used in low frequency small-signal measurement devices as a pre-amplifier such as EEG and ECG[23]. It is to note that as soon as the value of additional biasing resistance RA crosses 1KΩ, output waveforms become distorted with voltage and current goes below unity, Therefore, value of additional biasing resistance RA should not exceed 1KΩ.

Table 3: Effect of R_A on the Proposed amplifier

Performance Parameters	**Proposed Amplifier**	
	Without R_A (Under PSpice tool)	***With R_A (Under Cadence virtuoso tool)***
Amplifier current gain, A_{IGA}	0.010	1.22
Amplifier voltage gain, A_{VGA}	1.7493	117.493
Lower cut-off frequency, F_L	275.564 Hz	1.32 Hz
Upper cut-off frequency, F_H	21.207 MHz	201.002 KHz
Bandwidth, B_W	21.206 MHz	200.11 KHz
AC Current gain of the amplifier, $A_{IGA-RMS}$	0.010	---
AC Voltage gain of the amplifier, $A_{VGA-RMS}$	1.7483	---
Power gain, P_W in Watt	0.0174	143.341
Power gain, P_W in dB-Watt	-17.594	21.56
Phase Difference, $\theta°$	-164.599	-178.543
Device Current Gain, A_{IGD}	0.018	1.00
Device voltage Gain, A_{VGD}	1.9298	132.898
AC Current gain of the device, $A_{IGD-RMS}$	0.018	---
AC Voltage gain of the device, $A_{VGD-RMS}$	1.9298	---
Input Current IR_S	16.143 uA	12.86 uA
Load Current IR_L	167.394 nA	14.86 uA
Ratio, IR_L/IR_S	0.010	1.564
Input Voltage, V_1	1 mV	1 mV
Output Voltage, V_6	1.6768 mV	112.876 mV
Ratio, V_6/V_1	1.6783	112.876
Total Harmonics Distortion, THD	2.87%	32.87 u%

3.3. Effect of Optional biasing resistance R_{EX}

Performance of the proposed amplifiers have also been examined in the presence of optional biasing resistance R_{EX} under three distinct situations referred herein as Condition A, Condition B and Condition C. These conditions with their corresponding values of performance parameters have been stated below:

Condition A: When R_{EX}=150 MΩ is added between emitter of Q_1 to the collector of Q_2 and emitter of Q_1 is connected to terminal 4 in Figure 1 A under PSpice tool, it generates A_{IGA} =9.568, $A_{IGA\text{-}RMS}$ =9.568, A_{VGA} = 234.899, $A_{VGA\text{-}RMS}$ = 234.800, F_H = 3.7576 MHz, F_L = 39.276 Hz, B_W = 3.7575 MHz A_{IGD} = 17.694, $A_{IGD\text{-}RMS}$ = 17.694, A_{VGD} = 245.993, $A_{VGD\text{-}RMS}$ =245.993, P_G (in Watt) =2247.51, P_G (in dB-Watt) =33.517, V_1= 0.9991 mV, V_6 =240.808 mV, Ratio V_6/V_1 =241.024 , I(R_S) =2.3830 uA, I(R_L) = 24.078 uA, Ratio I(R_L)/I(R_S) =10.104, $\theta°$ = -177.692, and THD = 0.778%.

Parameters obtained in this condition is same as the standard parameters of the proposed amplifier stated in Table 2. However, bandwidth in this condition is lesser than the standard circuit (lower cut-off frequency F_L is higher and upper cut-off frequency F_H is lower)[24].

Similarly, when R_{EX}=10 KΩ is added between emitter of Q_1 to the collector of Q_2 and emitter of Q_1 is connected to terminal 4 in Figure 1 B under Cadence virtuoso tool, it produces voltage gain= 200.9616 F_H= 889.451 Hz, F_L=11.3185 Hz, B_W=876.321 Hz, current gain = 2.91 Device voltage= 306.302 Device current= 23.8 Phase of output voltage= -227.193 Phase margin =97.7038 Power spectral Density = 76.375 aV^2/Hz V_1=1mv V_0=-269.87 uV IR_S= 6.035uA IR_L= -21.534 Total Power Consumption= 125.4157 mW and THD=20.22 u%

Condition B: When R_{EX}=500 KΩ is directly added between emitter of Q_1 to the collector of Q_2 in Figure 1A, performance parameters are obtained which are as follows- A_{IGA} =2.2661, $A_{IGA\text{-}RMS}$ =2.2661, A_{VGA} =0.708, $A_{VGA\text{-}RMS}$ = 0.708, F_H = 11.705 MHz, F_L = 1.4968 Hz, B_W = 11.704 MHz A_{IGD} = 57836, $A_{IGD\text{-}RMS}$ = 57836, A_{VGD} = 0.797, $A_{VGD\text{-}RMS}$ =0.797, P_G (in Watt) =1.604, P_G (in dB-Watt) =2.052, V_1= 0.9991 mV, V_6 =0.705 mV, Ratio V_6/V_1 =0.706 , I(R_S) =31.131 nA, I(R_L) = 70.159 nA, Ratio I(R_L)/I(R_S) =2.259, $\theta°$ = 0.100, and THD = 0.709%.

Similarly, when R_{EX}= 10 KΩ is directly added between emitter of Q_1 to the collector of Q_2 in Figure 1B, performance parameters are obtained which are as follows- Voltage gain= 100.009, F_H=2.8 KHz Hz F_L=10.87 Hz B_W=2.6 KHz Current gain= 3.163 Device voltage= 0.993 Device current= 73.733K Phase of output voltage= -13.4979 Phase margin =97.7038 Power spectral

Density = 75.416 aV^2/Hz V_1=1mv V_0=-9.321 uV IR_S= 12 nA IR_L= 1.8457 nA Total Power Consumption= 3.028 mW THD= 35.46f %

Condition C: When emitter of Q_1 is directly connected to the collector of Q_2 with no R_{EX} in Figure 1A, it produces- A_{IGA} =3.1158, $A_{IGA-RMS}$ =3.1158, A_{VGA} =0.974, $A_{VGA-RMS}$ = 0.974, F_H = 183.582 MHz, F_L = 1.7128 Hz, B_W = 183.581 MHz A_{IGD} = 57837, $A_{IGD-RMS}$ = 57837, A_{VGD} = 0.984, $A_{VGD-RMS}$ =0.984, P_G (in Watt) =3.034, P_G (in dB-Watt) =4.8201, V_1= 0.9991 mV, V_6 =967.073 uV, Ratio V_6/V_1 =0.972 , I(R_S) =31.234 nA, I(R_L) = 97.159 nA, Ratio I(R_L)/I(R_S) =3.114, $\theta°$ = 0.118, and THD = 0.791%.

Similarly, when emitter of Q_1 is directly connected to the collector of Q_2 with no R_{EX} in Figure 1B, performance parameters remain same as found in Condition B.

It is to be mentioned that at R_{EX}< 500Ω, proposed amplifier (Figure 1A) becomes useless as the difference between the voltage gain in AC and transient analysis is much higher. Therefore, proper range of R_{EX} to receive faithful voltage amplification is $R_{EX} \geq$ 500Ω. Similarly, faithful range of operation for the proposed amplifier (Figure 1B) is 700Ω as the transient responses become distorted beyond this range[25].

3.4. Tuning Performance

Abhishek Motayed and S. Noor Mohammad had studied the tuning performance of BJT based Darlington pair small-signal amplifier for the very first time[25]. The same procedure has been adopted here to analyze the tuning performance of the proposed amplifier (Figure 1A) using PSpice tool. It is done under two conditions: (i) By varying emitter capacitance C_E and (ii) By varying load capacitance C_L keeping emitter capacitance C_E fixed at 100pF.

Variation of performance parameters of the proposed amplifier with respect to emitter capacitance C_E and load capacitance C_L has been recorded in Table 4 and Table 5 respectively.

Table 4 Variation of voltage gain, current gain and bandwidth with C_E

C_E	A_{IGA}	A_{VGA}	F_L	F_H	B_W
10pF	9.568	234.902	39.372 Hz	37.422 MHz	37.421 MHz
100pF	9.568	234.899	39.296 Hz	3.7218 MHz	3.7217 MHz
1nF	9.568	234.877	39.375 Hz	370.003 KHz	369.963 KHz
10nF	9.568	234.654	39.676 Hz	36.790 KHz	\36.750 KHz

Tuning performance for proposed amplifier with C_E is received for the range 10pF-10nF. Table 10 shows that change in bypass capacitor does not any change in voltage and current gain, but is plays the key role in adjusting the mid-band width. The bandwidth extends from 39.372 Hz to 37.422 MHz for

C_E=10pF, 39.296 Hz to 3.7218 MHz for C_E=100pF, 39.375 Hz to 370.003 MHz for C_E=10pF and 39.676 Hz to 36.790 KHz for C_E=10nF. Thus, while the lower limit of cut-off frequency merely changes to higher value, the upper limit of cut-off frequency shifts towards lower value with increasing bypass capacitor.

Table 5 Variation of voltage gain, current gain and bandwidth with C_L

C_L	A_{IGA}	A_{VGA}	F_L (Hz)	F_H (MHz)	B_W (MHz)
1fF	9.568	234.899	39.354	3.7310 MHz	3.7309 MHz
10fF	9.568	234.899	39.095	3.7704 MHz	3.7703 MHz
100fF	9.568	234.899	39.454	3.6847 MHz	3.6846 MHz
1pF	9.568	234.899	39.976	3.6802 MHz	3.6801 MHz
10pF	9.568	234.899	39.438	3.3808 MHz	3.3807 MHz
100pF	9.568	234.897	39.425	1.8293 MHz	1.8292 MHz
1nF	9.568	234.874	39.326	336.869 KHz	336.829 KHz
10nF	9.568	234.651	39.368	36.867 KHz	36.827 KHz

Refer Table 5. Tuning of proposed amplifier with C_L is obtained for variation between 1fF-10nF. Within this range, voltage and current gain remains constant, upper cut-off frequency shift from MHz to KHz and lower cut-off frequency merely shows any variation at increasing value of C_L[26].

Thus, increase in C_E causes lower cut-off frequency to higher value and increase in C_L causes upper cut-off frequency to lower value, therefore their proper adjustment, can, therefore lead to such a tuning that frequency response of the amplifier peak around a frequency of desired frequency and fall off on both side of frequency. This is shown in Fig. 8. with two combinations of C_E and C_L – (i) C_E=1pF, C_L=1nF and (ii) C_E=0.01UF, C_L=10nF

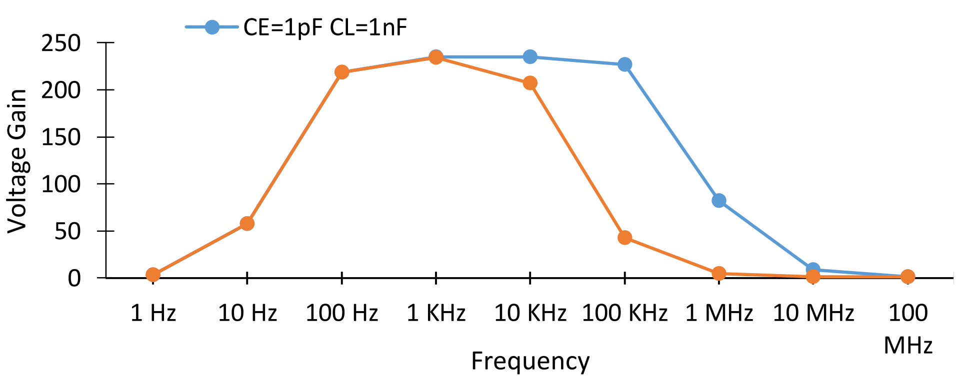


Figure 4. Tuning performance of the proposed amplifier (Figure 1A)

Similarly, tuning of the reference amplifier with C_E and C_L is obtained for the variation within the range 10pF-100nF and 1pF-10nF respectively[16].

3.5. Noise Sensitivity

Noise energy always available due to the presence of active and passive components within the circuit, and therefore plays the important role as a liming factor for the determination of operational signal levels in a circuit[23]. It therefore becomes necessary to study and analyze the noise present in the circuit for a better performance, as it potentially affects the performance of the circuit as well as the quality of the output[24].

Input and output noises for the proposed amplifier (Figure 1A) at 1KHz and 1MHz operating frequencies within the temperature range -30°C ≤ T ≤ +80°C has been examined using PSpice tool and recorded in Table 6. Input noise of the proposed amplifier increases with the rise of temperature at 1KHz and 1MHz frequencies and output noise at 1MHz frequency increase with increasing temperature. However, output noise at 1KHz frequency increases up to room temperature 27°C and decreases thereafter. It has also been observed that output noise is higher than input noise at both frequencies. It must be noted that at 1KHz operating frequency and room temperature, output noise of proposed amplifier (10^{-9} V/Hz) is lower than reference amplifier (10^{-7} V/Hz)[25].

Table 6 Noise Analysis of Proposed amplifier

Temp (°C)	At 1 KHz Frequency		At 1 MHz Frequency	
	NN_{OUT} (10^{-9} V/Hz)	N_{IN} (10^{-12} V/Hz)	N_{OUT} (10^{-9} V/Hz)	N_{IN} (10^{-12} V/Hz)
-30	54.240	211.817	44.634	180.395
-10	54.334	218.917	45.202	188.522
0	54.266	222.424	45.451	192.504
10	54.386	225.904	45.679	196.436
27	54.399	231.760	46.022	203.015
50	54.290	239.573	46.401	211.721
80	54.196	249.587	46.768	222.766

Similarly, for reference amplifier, Input and output noises increase with temperature except the output noise at 1 MHz, which unusually starts decreasing beyond 10C[16]. Since the level of input and output noises for reference and proposed amplifier are low enough and within the permissible limit, therefore both the amplifiers could be used as 'high gain low noise low THD wideband amplifier' for various applications of electronics and communication.

3.6. Temperature Effect

Variation of performance parameters of the proposed amplifier (Figure 1A) with respect to temperature has been listed in Table 7. In case of proposed amplifier, all the performance parameters decrease with temperature elevation except bandwidth, which unexpectedly withstands sudden increment at 27℃, decreases with increasing temperature. This declination in voltage and current gain is perhaps due to rise of collector-base leakage current of third BJT with rising temperature which in-turn elevates the collector current and caused lowering of output voltage and current[26].

Table 7 Temperature Effect of Proposed amplifier

Performance Parameter	**Temperature in ℃**						
	-30	***-10***	***0***	***10***	***27***	***50***	***80***
A_{IGA}	9.673	9.638	9.620	9.601	9.568	9.521	9.4523
A_{VGA}	256.294	248.399	244.616	240.936	234.899	227.131	217.602
F_L	42.681 Hz	41.892 Hz	41.039 Hz	`40.073 Hz	39.076 Hz	38.240 Hz	36.947 Hz
F_H	3.7386 MHz	3.7276 MHz	3.4860 MHz	3.5820 MHz	3.8127 MHz	3.7181 MHz	3.7170 MHz
B_W	3.7385 MHz	3.7275 MHz	3.4859 MHz	3.5819 MHz	3.8126 MHz	3.7180 MHz	3.7169 MHz
A_{IGD}	17.870	17.812	17.782	17.750	17.694	17.612	17.495
A_{VGD}	267.528	259.561	255.752	252.051	245.993	238.225	228.745
P_W dB-Watt	33.942	33.791	33.716	33.642	33.517	33.345	33.131
Phase	-177.514	-177.600	-177.631	-177.642	-177.692	-177.755	-177.832
THD	0.801%	0.793%	0.789%	0.785%	0.778%	0.765%	0.757%

3.7. Phase Variation

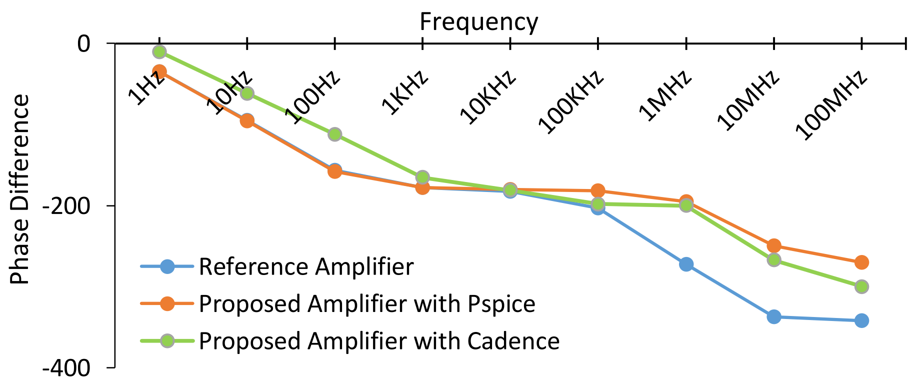


Figure 5. Phase variation of the amplifiers

Variation of phase-difference of output current with respect to frequency for reference and proposed amplifiers using PSpice and Cadence virtuoso tool has been shown in Figure 5[21]. Output current phase difference of all the amplifiers decreases with increasing frequency. It is also found that at 1KHz operational frequency, phase-difference of output current of proposed amplifier under Cadence virtuoso tool (-165.27^{o}) is higher as compared to all the other amplifier[16].

3.8. Effect of DC Supply Voltage

Variation of voltage gain of reference and proposed amplifiers with respect to DC supply voltage has been depicted in Figure 6. Voltage gain of the proposed amplifier increases non-linearly within the range 5 Volt $\leq V_{CC} \leq$ 30 Volt for Figure 1A and 1 Volt $\leq V_{CC} \leq$ 18 Volt for Figure 1 B and decreases thereafter whereas it is observed zero for $V_{CC} \leq$ 5 Volt for Figure 1A. Hence the faithful amplification range of V_{CC} for proposed amplifiers is 5-30 Volt and 1-18 Volt for Figure 1A and Figure 1B respectively. Similarly, for reference amplifier, voltage gain is observed zero between 0 Volt $\leq V_{CC} \leq$ 4 Volt, increases almost non-linearly between 4 Volt $\leq V_{CC} \leq$ 40 Volt. and thereafter, the amplifier does not respond properly. Hence, permissible range for the reproduction of amplified output at different V_{CC} is 4-40 Volt[16].

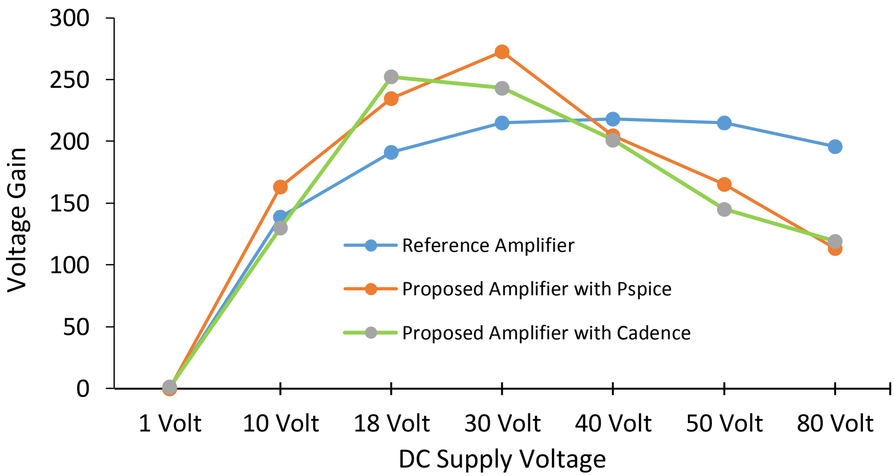


Figure 8. Variation of voltage gain with V_{CC}

As a matter of fact, at both reference and proposed amplifier possess high V_D at node 3 which generally increases with increasing V_{CC} up to 30 volts for reference amplifier and 40 volts for proposed amplifier and decreases afterwards. This causes significant declination in the voltage gain of both amplifiers[16].

3.9. Effect of R_1, R_2, R_C, R_L and R_S

Table 8 shows the performance parameters of both amplifiers at maximum and minimum values of R_1 and R_2. It is found that proposed amplifier produces undistorted outputs for 7KΩ-1MΩ range of R_1 and 10KΩ-250KΩ range of R_2. Similarly, the permissible range of resistance R_1 for reference amplifier is 6.6KΩ-200KΩ whereas this for R_2 is 66KΩ- 380KΩ for suitable biasing and purposeful amplification.

Table 8 Performance parameters at limiting values of R_1 and R_2

Parameters	**R_1**		**R_2**	
	Min at 7KΩ	**Max at 1MΩ**	**Min at 10KΩ**	**Max at 250KΩ**
A_{IGA}	7.5644	0.278	903e-6	8.5963
A_{VGA}	111.128	130.008	1.2801	116.122
F_L	23.829 Hz	748.904 Hz	2.2636 KHz	21.847 Hz
F_H	1.9134 MHz	5.0178 MHz	9.967 MHz	2.1622 MHz
B_W	1.9133 MHz	5.0177 MHz	9.964 MHz	2.1621 MHz

Table 9 lists the variation of voltage gain of proposed amplifier with R_L and R_C. It can be explained that at R_L=33KΩ, 47KΩ and 66KΩ, voltage gain increases for increasing value of R_C up to R_C=33KΩ and decreases afterwards. Similarly, at R_L=5KΩ, 10KΩ, voltage gain rises with increasing R_C up to R_C=12K R_L=33KΩ, 47KΩ and decreases beyond this value. In the same way, for R_L=1KΩ, 100KΩ voltage gain increases with increasing R_C up to R_C=5K and R_C=47KΩ respectively and decreases thereafter.
Contrarily, Voltage gain of the reference amplifier increases from a certain minimum value until it tends towards saturation beyond R_L=33KΩ corresponding to every value of R_C[16].

Table 9 Variation of Voltage gain with R_L& R_C

R_L	**Voltage gains of Proposed amplifier at distinct values of R_C**						
	1KΩ	**5KΩ**	**12KΩ**	**33KΩ**	**47KΩ**	**66KΩ**	**100KΩ**
1 KΩ	133.127	*158.148	152.415	128.365	115.622	101.847	83.965
5 KΩ	166.033	215.837	*221.576	213.566	206.571	197.399	182.601
10 KΩ	171.326	226.148	*234.899	232.888	229.098	223.624	214.030
33KΩ	175.219	233.938	245.174	*248.561	247.942	246.444	243.205
47 KΩ	175.736	234.986	246.571	*250.747	250.612	249.745	247.575
66 KΩ	176.089	235.703	247.528	*252.252	252.456	252.035	250.632
100 KΩ	176.387	236.309	248.339	253.532	*254.029	253.994	253.261

Performance parameters of the proposed amplifier has also been studied with the varying range of source resistance R_S and listed in Table 10. It has been found that variation in base resistance does not bring any change in current gain whereas voltage gain decreases with increasing R_S. Bandwidth, THD, I_{RS} and I_{RL} of the proposed amplifier decreases with increasing R_S.

Table 10 Variation of Performance parameters with R_S

R_S	A_{VGA}	F_H	F_L	B_W	A_{IGA}	THD	I_{RS}	I_{RL}
1Ω	234.899	3.8127 MHz	39.076 Hz	3.8126 MHz	9.568	0.778%	2.3880 uA	24.085 uA
100Ω	188.972	3.5428 MHz	31.553 Hz	3.5427 MHz	9.568	0.776%	1.9273 uA	19.290 uA
200Ω	157.806	3.3513 MHz	27.740 Hz	3.3512 MHz	9.568	0.775%	1.6133 uA	16.058 uA
500Ω	105.572	2.8911 MHz	17.872 Hz	2.8910 MHz	9.568	0.776%	1.0824 uA	10.661 uA
700Ω	86.487	2.7745 MHz	14.588 Hz	2.7744 MHz	9.568	0.778%	889.380 nA	8.7041 uA
1KΩ	68.037	2.7327 MHz	11.627 Hz	2.7326 MHz	9.568	0.780%	701.148 nA	6.8500 uA
3KΩ	28.090	2.4141 MHz	5.0983 Hz	2.4140 MHz	9.568	0.784%	291.881 nA	2.8112 uA
5KΩ	17.698	2.3513 MHz	3.5552 Hz	2.3512 MHz	9.568	0.788%	183.445 nA	1.7725 uA
7KΩ	12.919	2.3089 MHz	2.8685 Hz	2.3088 MHz	9.568	0.789%	134.024 nA	1.2946 uA

Adversely, in reference amplifier, maximum of the A_{VG} is received for lower values of R_S. A_{VG} reaches to 384.46 for R_S=10Ω and dips to 10.05 at R_S=7KΩ. Simultaneously, load current I_{RL}, I_{RS}, F_H, F_L and bandwidth of the proposed amplifier also reduces with elevation in R_S. However, THD reduces up to 1KΩ but suddenly shoot-up at 3KΩ and thereafter reduces further at higher R_S values[16].

Refer Table 10. Proposed amplifier within the range 3KΩ-7KΩ of R_S with low F_L within the range 2.8685 Hz-5.0983 Hz, low THD and very low order input and output current may be used in the preamplifier stages for the amplification of PPG signals (Photoplethysmography) which is generally ranging between 0.5-4 Hz for monitoring the shape of the blood pressure signal[17,18]. Block diagram is shown in Figure 9.

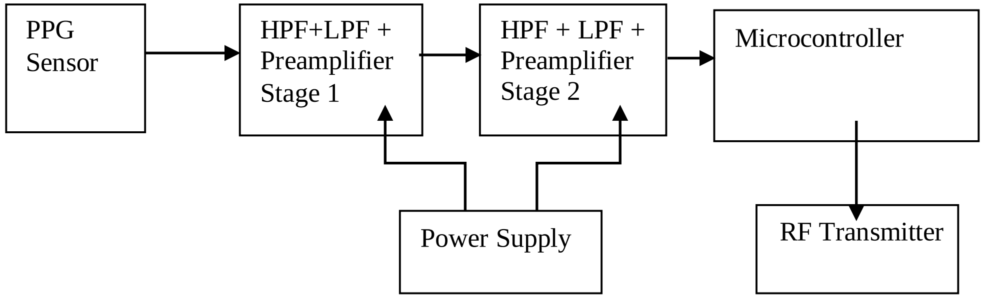


Figure 9. Block diagram of proposed amplifiers in PPG signal application

3.10. Effect of β variation on Proposed Amplifier

Table 11, Table 12 and Table 13 describes the variation of the performance parameters at identical values of β_1, β_2 and β_3; fixed β_2 at 240, varying β_1 and β_3 and fixed β_1 and β_3 at 240 and varying β_2 respectively[19,20].

Refer Table 11. When β_1, β_2 and β_3 is increased with identical values, amplifier current gain and device current gain primarily increases and suddenly shoots up at $\beta_1= \beta_2 =\beta_3=50$. At $\beta_1= \beta_2 =\beta_3=100$ it again drops to a minimum value afterwards it increases up to $\beta_1= \beta_2 =\beta_3=250$ and decreases thereafter. Similarly, amplifier voltage gain and device voltage gain initially increases and undergoes sudden increment at $\beta_1= \beta_2 =\beta_3=50$. At $\beta_1= \beta_2 =\beta_3=100$, it again decreases thereafter it gradually increases up to $\beta_1= \beta_2 =\beta_3=240$ and decreases beyond this range. Bandwidth decreases with increasing β_1, β_2, β_3 whereas THD decreases up to $\beta_1= \beta_2 =\beta_3=240$ and increases afterwards.

Table 11 Performance parameters at identical values of β_1, β_2 and β_3

Performance Parameters	**β_1=β_2 = β_3= 5**	**β_1= β_2= β_3= 50**	**β_1=β_2 = β_3= 100**	**β_1=β_2 = β_3= 150**	**β_1=β_2 = β_3= 200**	**β_1= β_2= β_3= 240**	**β_1= β_2= β_3= 250**	**β_1= β_2= β_3= 300**	**Performance Parameters**	**β_1=β_2 = β_3= 5**
A_{IGA}	110e-6	168.450	4.0629	6.1486	8.1585	9.568	9.701	0.101	A_{IGA}	110e-6
A_{IGD} (Simulated Value)	170e-6	303.239	7.4372	11.310	15.056	17.694	17.947	0.184	A_{IGD} (Simulated Value)	170e-6
A_{IGD} (Theoretical Value)	125	125000	1000000	3375000	8000000	13824000	15625000	27000000	A_{IGD} (Theoretical Value)	125
% Variation of A_{IGD}	99.99 %	99.75 %	99.99 %	99.99 %	99.99 %	99.99%	99.99%	99.99%	% Variation of A_{IGD}	99.99 %
A_{VGA}	0.006	14343	151.156	193.057	221.738	234.899	232.533	74.182	A_{VGA}	0.006
F_L (Hz)	80.535 Hz	17.826 MHz	60.767 Hz	50.051 Hz	43.466 Hz	39.076 Hz	38.480 Hz	1.1773 KHz	F_L (Hz)	80.535 Hz
F_H (MHz)	187.717 MHz	33.844 MHz	3.4574 MHz	3.6531 MHz	3.7357 MHz	3.8127 MHz	3.7119 MHz	6.4662 MHz	F_H (MHz)	187.717 MHz
B_W (MHz)	187.716 MHz	33.843 MHz	3.4573 MHz	3.6530 MHz	3.7356 MHz	3.8126 MHz	3.7118 MHz	6.4650 MHz	B_W (MHz)	187.716 MHz

Refer Table 12. Up to β1= β3 = 100 and β2 =240 amplifier/device voltage and current gain changes in zig-zag manner. From β1= β3 = 150 to β1= β3 = 250 (Keeping β2 fixed at 240) amplifier and device current gain increases and decreases beyond this range whereas amplifier and device voltage gain increases from β1= β3 = 150 to β1= β3 = 240 and decreases thereafter.

Bandwidth also decreases up to β1= β3 = 200 and thereafter changes in zig-zag manner. Instead, THD decreases up to β1= β3 = 240 and increases beyond this range.
Refer Table 13. When β1 and β3 is fixed at 240 and β2 is varied up to 300, all the performance parameters remain constant whereas bandwidth changes in zig-zag manner.
It is very important to note that up to β1= β2 =β3=70, proposed amplifier remains impractical because large difference is observed between voltage gain under AC and transient analysis. Hence, to achieve faithful amplification values of β1, β2, β3 should always be taken greater than 70.

Table 12 Performance parameters at fixed β_2 and varying β_1, β_3

Performance Parameters	**$\beta_1=\beta_3=5$ $\beta_2=240$**	**$\beta_1=\beta_3=50$ $\beta_2=240$**	**$\beta_1=\beta_3=100$ $\beta_2=240$**	**$\beta_1=\beta_3=150$ $\beta_2=240$**	**$\beta_1=\beta_3=200$ $\beta_2=240$**	**$\beta_1=\beta_3=240$ $\beta_2=240$**	**$\beta_1=\beta_3=250$ $\beta_2=240$**	**$\beta_1=\beta_3=300$ $\beta_2=240$**
A_{IGA}	110e-6	169.241	4.0628	6.1486	8.1585	9.568	9.701	0.101
A_{IGD} (Simulated Value)	170e-6	304.663	7.4371	11.310	15.056	17.694	17.947	0.184
A_{IGD} (Theoretical Value)	6000	600000	2400000	5400000	9600000	13824000	25000000	21600000
% Variation of A_{IGD}	99.99%	99.94%	99.99%	99.99%	99.99%	99.99%	99.99%	99.99%
A_{VGA}	0.006	14413	151.154	193.057	221.738	234.899	232.532	74.177
F_L (Hz)	80.535 Hz	17.768 MHz	59.616 Hz	50.013 Hz	43.476 Hz	39.076 Hz	38.676 Hz	1.7006 KHz
F_H (MHz)	187.717 MHz	34.117 MHz	3.4847 MHz	3.6844 MHz	3.7191 MHz	3.8127 MHz	3.7229 MHz	6.4770 MHz
B_W (MHz)	187.716 MHz	34.116 MHz	3.4846 MHz	3.6843 MHz	3.7190 MHz	3.8126 MHz	3.7228 MHz	6.4752 MHz
A_{VGD}	0.009	14480	157.153	200.364	230.425	245.993	245.822	85.323
THD	14.72%	1.21%	1.097%	0.969%	0.907%	0.778%	1.05%	29.61%

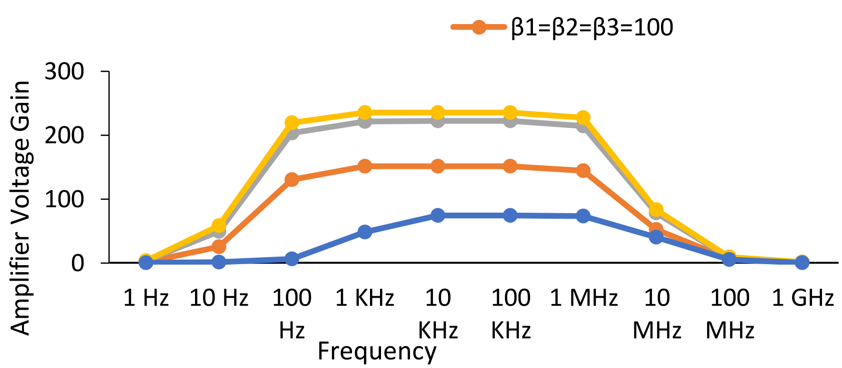


Figure 9. Variation of voltage gain with identical values of β_1, β_2 and β_3

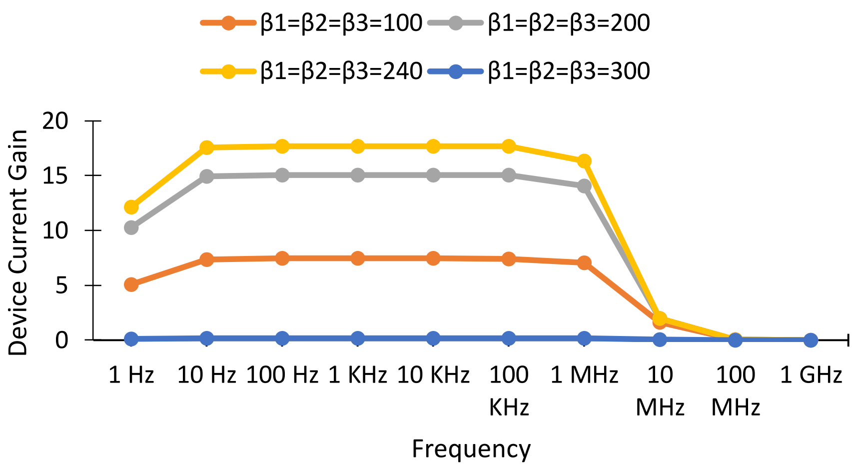


Figure 10. Variation of Device Current gain with identical values of β_1, β_2 and β_3

Figure 9 and Figure 10 describes the variation of amplifier voltage gain and device current gain with identical range of β1, β2 and β3. Clearly, maximum values of respective performance parameters in both graphs are attained at β1=β2=β3=240 and minimum values are obtained at β1=β2=β3=300. Therefore, value of β in each transistor are kept 240.

Table 13 Performance parameters at varying β_2 and fixed β_1, β_3

Performance Parameters	**β_1=β_3=240 β_2= 5**	**β_1=β_3=240 β_2= 50**	**β_1=β_3=240 β_2= 100**	**β_1=β_3=240 β_2= 150**	**β_1=β_3=240 β_2= 200**	**β_1=β_3=240 β_2= 240**	**β_1=β_3=240 β_2= 250**	**β_1=β_3=240 β_2= 300**
A_{IGA}	9.563	9.568	9.568	9.568	9.568	9.568	9.568	9.568
A_{IGD} (Simulated Value)	17.683	17.693	17.693	17.694	17.694	17.694	17.694	17.694
A_{IGD} (Theoretical Value)	288000	2880000	5760000	8640000	11520000	13824000	14400000	17280000
% Variation of A_{IGD}	99.99%	99.99%	99.99%	99.99%	99.99%	99.99%	99.99%	99.99%
A_{VGA}	234.759	234.880	234.892	234.896	234.898	234.899	234.899	234.900
F_L (Hz)	39.447 Hz	39.628 Hz	39.432 Hz	39.428 Hz	39.604 Hz	39.076 Hz	39.427 Hz	39.423 Hz
F_H (MHz)	3.6848 MHz	3.7545 MHz	3.7561 MHz	3.7499 MHz	3.7720 MHz	3.8127 MHz	3.7261 MHz	3.6740 MHz
B_W (MHz)	3.6847 MHz	3.7544 MHz	3.7560 MHz	3.7498 MHz	3.7719 MHz	3.8126 MHz	3.7260 MHz	3.6739 MHz
A_{VGD}	245.899	245.981	245.989	245.991	245.993	245.993	245.994	245.994
THD	0.779%	0.777%	0.778%	0.778%	0.778%	0.778%	0.778%	0.778%

3.11. AC Equivalent Circuit

Small-signal equivalent model of the proposed amplifier is sketched in Figure 11.

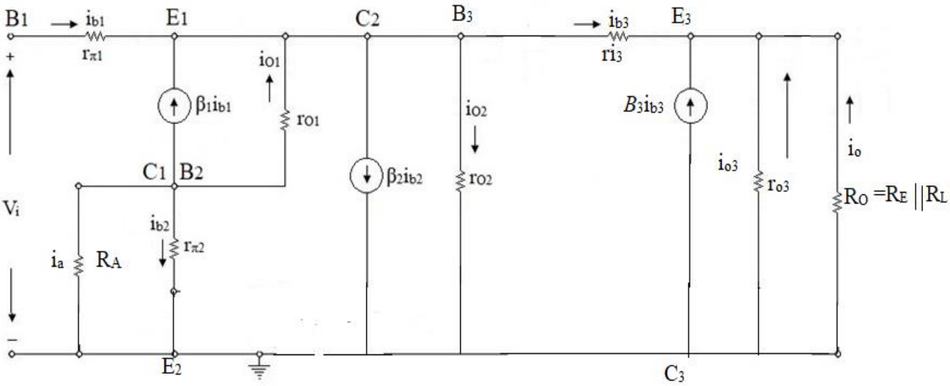


Figure 11. Small-signal AC model of the proposed amplifier

Simulation of the proposed amplifier circuit realizes β_1=240, β_2=240, β_3=240, $r_{\pi1}$=170Ω, $r_{\pi2}$=194Ω, $r_{\pi3}$=51.4KΩ, r_{O1}=1TΩ, r_{O2}=88.9Ω and r_{O3}=997GΩ Since r_{O1} and r_{O3} of the proposed amplifier is high and can be ignored during analysis. The reduced figure is shown in Figure 12.

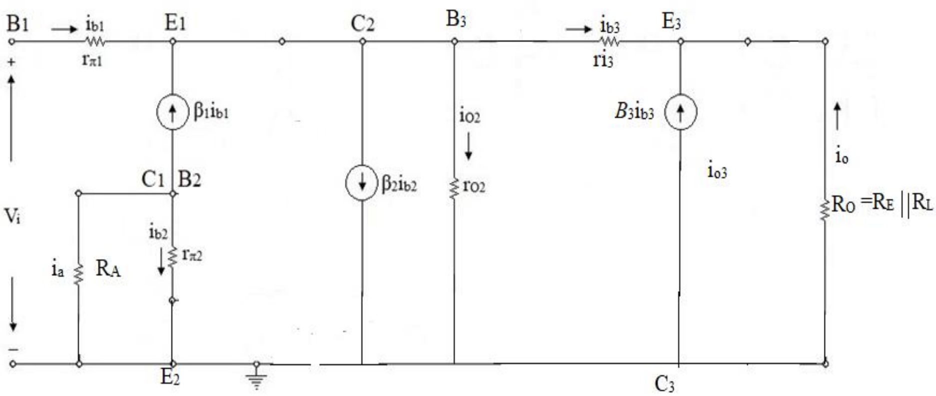


Figure 12. Modified small-signal AC model of the proposed amplifier

According to Kirchoff's Current law (KCL), current entring the node must be equal to the current leaving the node. Applying this law at node E_1,

$$ib_1 + \beta_1 ib_1 - \beta_2 ib_2 + \beta_3 ib_3 - ib_3 - i_{o2} = i_o$$

(1) $$i_o = ib_1(1+\beta_1) - ib_3(1-\beta_3) - \beta_2 ib_2 - i_{o2}$$

Applying this law at node E_2,

$$ib_2 + i_a + \beta_2 ib_2 = 0$$

(2) $$i_a = -ib_2(1+\beta_2)$$

Similarly, at node B_2 or C_1,

$$ib_2 + i_a + \beta_1 ib_1 = 0$$

(3) $$ib_1 = \frac{-(i_a+ib_2)}{\beta_1}$$

Since $A_{IG} = \frac{i_o}{ib_1} = \frac{ib_1(1+\beta_1)-\beta_2 ib_2 - ib_3(1-\beta_3)-io_2}{\frac{-(i_a+ib_2)}{\beta_1}}$

Hence expression for current gain may be given as

$$A_{IG} = \frac{-\beta_1\{ib_1(1+\beta_1)-\beta_2 ib_2 - ib_3(1-\beta_3)-io_2\}}{(i_a+ib_2)}$$

3.12. Layout and Post-layout Simulation results

Layout of the proposed amplifier has been made using Cadence virtuoso tool at 180nm technology under Layout XL editor window[25,26].

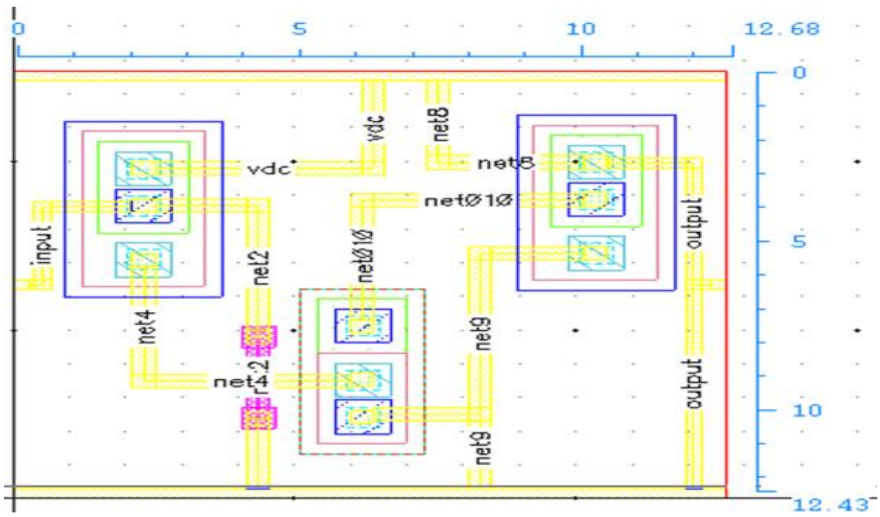


Figure 13. Layout of the proposed amplifier(dimensions 12.68µm x 12.43 µm)

Figure 13 shows that the layout of the proposed amplifier takes up small area of 157.6124 µm^2 (12.68µm×12.43 µm). Input pin, output pin, DC supply voltage pin and ground pin have been kept at left, right, top and bottom corners respectively. Horizontal rail have been applied at DC supply pin and ground for better connections among the wires. Here, yellow wire respresents metal wire while pink wire represents poly wire. No errors have been found during Design Rule Check(DRC) and Layout vs Schematic (LVS) runs. The values of parasitic resistance and capacitance have been collected after DRC and LVS run and transferred to amplifier circuit netlist for performing post layout simulation[23]. A comparison table of the performance parameters of the proposed amplifier before and after layout have been shown in Table 14 . Slight variations are observed in the values of performance parameters before and after layout, which validate our design in 180nm technology.

Table 14 Comparison between pre-layout and post-layout simulation results

Performance Parameters	**Pre-Layout Simulation Results**	**Post-Layout Simulation Results**
Amplifier Voltage Gain A_{VGA}	252.106	245.337
Upper Cut Off Frequency F_H (for A_{VGA})	212.598 MHz	212.761 MHz
Lower Cut Off Frequency F_L (for A_{VGA})	234.786 Hz	231.516 Hz
Band-Width B_W (for A_{VGA})	212.597 MHz	212.760 MHz
Unity Gain Band-Width (for A_{VGA})	23.5332 GHz	25.3190 GHz
Amplifier Current Gain A_{IGA}	7.6838	6.433
Upper Cut Off Frequency F_H (for A_{IGA})	5.64905 MHz	5.790 MHz
Lower Cut Off Frequency F_L (for A_{IGA})	230.958 Hz	229 .221 Hz
Band-Width B_W (for A_{IGA})	5.6488 MHz	5.7897 MHz
Device Voltage Gain A_{VGD}	356.459 (Distortion)	349.90
Device Current Gain A_{IGD}	7.6977	7.005
Power Gain P_A (in dB-Watt)	32.871	31.981
Output Voltage Phase Difference θ^O	-165.27	-165.754
Phase Margin θ_M of Voltage gain	158.914	161.53
Total Harmonic Distortion THD	25.3027 u%	26.703 u%
Total Power Consumption, P_W	119.596 mW	112.592 mW
Input Signal Voltage	1mV at 1KHz	1mV at 1KHz
Permissible Range of Input Signal Voltage	10 nV-1 uV	10 nV-1 uV
Slew rate of output voltage	1.3 V/ms	1.26 V/ms
Current across Source Resistance I_{RS}	6.339 uA	5.394 uA
Current across Load Resistance I_{RL}	39.22 uA	38.22 uA
Voltage across source resistance V_{RS}	1 mV	1 mV
Voltage across load resistance V_{RL}	196.099 mV	192.05 mV
Power Spectral Density	3.1742 fV^2/Hz	3.0713 fV^2/Hz
Input Noise	223.95 pV/sqrt (Hz)	226.45 pV/sqrt (Hz)
Output Noise	55.059 nV/ sqrt (Hz)	53.935 nV/sqrt (Hz)
Transfer Function	252.105 V/V	245.337 V/V
Chip Area	12.62 μm × 12.74 μm	----

Figure 14 shows the graphical representation of the performance parameters to have a more clear view of how the values of voltage gain, current gain and total power consumption changes after layout. The values represented on the graphs for the parameters have been deduced during ac-analysis before and after layout in 180nm technologies in Cadence virtuoso tool[21-23].

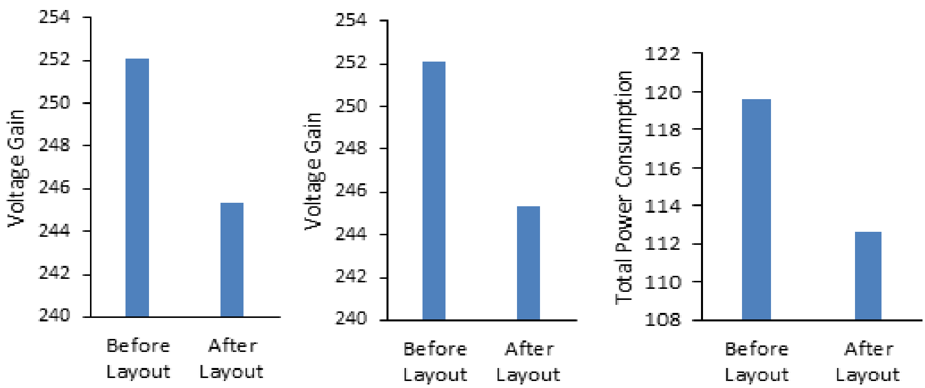


Figure 14. Graphical representation of parameters of the proposed amplifier before and after layout

Here the X-axis represents the condition of simulation and Y-axis represents the values performance parameters in 180nm technologies. The graphs have almost same values for all the parameters before and after layout.

5. Conclusion

Modified versions of PNP Sziklai pair small-signal amplifer under triple transistor topology has been proposed and analyzed in the present paper using PSpice and Cadence virtuoso tool at 180nm technology. The parameters of proposed amplifier are nearly same before and after layout, thus it verifies the proposed designs in 180nm technology. Resulting small power dissipation the proposed amplifiers also remove the poor response problem of small-signal Darlington pair amplifier at higher frequencies and narrow-bandwidth restrictions of small-signal PNP and NPN Sziklai pair amplifiers. Proper adjustment of C_E and C_L leads to a tuning of the proposed as well as reference amplifier at a desired frequency of a specific channel which shows their application in small signal receiver stages.

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