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A New Topology for Low Voltage Level Shifted Cascode Current Mirror*

Ganga Ram Mishra
Department of Electronics Engg., Amity School of Engg. & Technology
Amity University Uttar Pradesh Lucknow Campus

Raj Kumar Tiwari
Circuit Design and Simulation Lab, Department of Physics and Electronics
Dr. R. M. L. Avadh University Faizabad (U.P.), India

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Abstract: The Current mirrors are the core structure for almost all analog and mixed mode circuits. The performance of the analog structures depends on the performance of current mirror, which largely depends on their characteristics. For low voltage design circuit, low voltage currents mirrors are mandatory with high performance. In this paper we present a new topology for a simple high performance current mirror for low voltage applications .This structure is simulated using SPICE simulator for 0.15 micron CMOS technology.

1. Introduction

With the rapid growth of portable consumer electronics, computers and communications, more and more chips are required to have small size, low power and wide dynamic range[1]. So, low power and low voltage analog and mixed mode circuits are gaining importance. For a low voltage and high performance analog and mixed mode circuit design current mode design technique is a better choice[2]. In current mode circuit design the designer have more concern with the current levels for the operation of circuit. In the current mode circuit design the current mirrors are the core structure for almost all analog and mixed mode circuits. The performance of the analog circuit depends on the performance of current mirror, which largely depends on their characteristics. For low voltage design circuit, low voltage currents mirrors are mandatory with high performance[3-8]. The accuracy, output impedance and large output voltage signal swing are the most important parameter to determine the performance of the current mirror. In high speed applications, the settling time of current mirror is another important parameter[9]. The cascode current mirror, the Wilson current mirror and the

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regulated cascode current mirror are widely used current mirrors[10-11]. However, they are not suitable for low voltage applications due to their limited signal swing. So, Low voltage cascode current mirrors have received considerable attention due to their large output voltage swing and small input voltage compared to a conventional cascode current mirror[12]. This is a most useful property in low voltage/low power analog circuit design. However, as the low voltage current mirror uses a fixed bias voltage for the cascode transistor the dynamic range of the current mirror is limited when both the mirror input transistor and the cascode input transistor are required to stay in saturation. At high input currents the drain-source voltage of the mirror transistors decreases and eventually they will enter the linear region.

Most of the current mirror reported though[8-13] has high output voltage signal swing; they require a minimum input voltage. This voltage is due to the traditional diode connected configuration of the input MOSFET. In present paper we propose a new topology for low voltage and high performance current mirror which uses cascading approach for increasing output impedance and level shifting approach for reduction of power. The proposed circuit is simulated using SPICE simulator for 0.15 micron CMOS technology.

2. Basic Current Mirror

A basic current mirror is shown in figure 1. It is composed of two transistors, of which one, M1is diode-connected. M1 receives the reference current Iref and measures it by developing at its gate the voltage VGS1 this voltage biases the gate of M2.

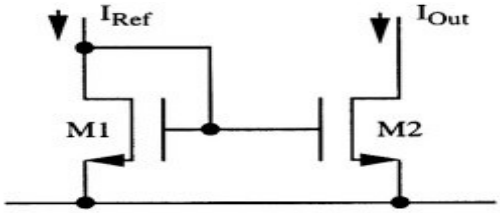

Figure 1: Simple Current mirror

Both transistors operate in the saturation region; therefore, the currents are

$$I_{Ref} = I_1 = \frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_1 \left(V_{GS1} - V_{Th}\right)^2 \left(1 + \lambda V_{DS1}\right)$$

$$I_{Out} =$$

The output resistance of the current mirror at any given operating point is expressed as

$$R_0 = r_{02} = \frac{1}{\lambda I_{D_2}},$$

where R_O is output resistance of current mirror, ro_2 is resistance across MOS transistor M2, λ is channel length modulation and I_{D2} the drain current of M2 which is the output current. Unfortunately, the value of output resistance which can be achieved with the technologies and medium value currents used is not large enough for a number of applications. For low voltage applications the simple scheme in Fig. 1 may be preferred because of its excellent output dynamic range, whereas this structure of current mirror results in significant error in copying currents due to effect of channel length modulation, threshold offset between the two transistors and imperfect geometrical matching.

3. Cascode Current Mirror

The cascode current mirror is widely used in MOS technology. It is the cascode connection of a common source and a common gate stage.

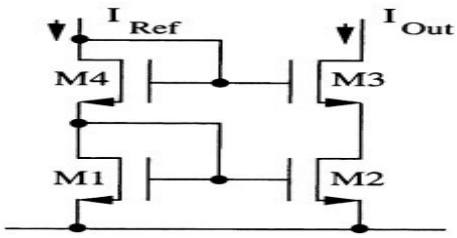

Figure 2: Casode Current mirror

The idea behind cascode structure is to convert the input voltage to a current and apply the result to a common source stage. Figure 2 shows basic cascode current mirror configuration. The output stage consists of two transistors M2 and M3 in the cascode arrangement. Their biases result from two other transistors M1 and M4 which are diode-connected[14-16].The output impedance increases because of the cascode arrangement. The output impedance of the cascade structure is expressed as

$$V_{out} > V_{DS2} + V_{eff} = 2V_{eff} + V_{th}.$$

Since g_{ds3} is very small, it can be neglected, so we get

$$r_{out} \cong r_{ds3}[1 + r_{ds2}(g_{m3} + g_{s3})].$$

This equation further approximated as

$$r_{out} \cong r_{ds3}(r_{ds2}\, g_{m3}\ ).$$

Thus the output impedance has been increased by a factor of $r_{ds2}\, g_{m3}$ and will depend on the transistor sizes, currents and the technology used. But in the cascode configuration the increased output resistance is paid for by reduction of the output dynamic range. Since the n-channel transistor operates in saturation region if its drain-source voltage is greater than V_{eff}, which is possible if

$$V_{eff} = V_{GS} - V_{in}$$

and V_{eff} is given as

$$V_{eff} = \sqrt{\frac{2l_D}{\mu_n C_{ox}(W/L)}}.$$

If we assume all transistors have the same sizes and currents, then all have same V_{eff} and thus same gate-source voltages. So,

$$V_{G4} = V_{GS1} + V_{GS4} = 2V_{eff} + V_{th}$$

and

$$V_{DS2} = V_{G4} - V_{GS3} = V_{G4} - (V_{eff} + V_{th}) = V_{eff} + V_{th}.$$

Thus, the drain-source voltage of M2 is larger than the minimum needed to place it at the edge of the saturation. Generally the drain-source voltage of M2 is V_{th}, which is taken larger than that is required. The minimum allowed output voltage is expressed as

$$V_{out} > V_{DS2} + V_{eff} = 2V_{eff} + V_{th}.$$

Thus, the minimum output voltage cannot be less than one threshold plus two saturation voltages. This is a serious disadvantage of cascade structure and can be used where the output impedance is a major factor for design. Since cascoding structure increases the voltage gain of amplifier and the output impedance of current sources. It also provides shielding of the bottom transistor. There are two main advantages of using cascode structures. It provides higher output impedance and reduces the effect of miller capacitance on the input of the amplifier. This approach of current mirror results in a very high gain stage and widely used in op-amps, along with low power dissipation.

4. Low Voltage Current Mirror

The low voltage operation is a key requirement especially for battery operated circuits. Therefore, current mirrors must ensure the highest output swing together with a high output resistance, even if we have to sacrifice for this result the beneficial systematic match between the reference and generated current [23]. In achieving this compromise solution, we can observe that the output impedance remains quite high so long as the two transistors in the cascode configuration are in saturation. A level shifting approach is one of the most widely used techniques for decreasing the voltage level at the input stage of the current mirror. The level shifted current mirror is drawn in figure 3 .The transistor M3 shifts the voltage level at the drain terminal of M1.

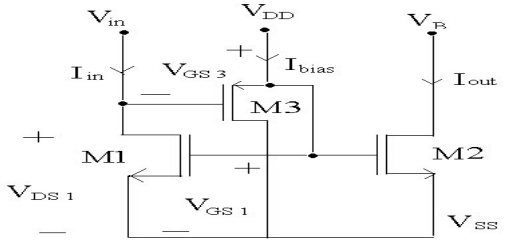

Figure 3: Level Shifted Current mirror

A Low Voltage Current Mirror (LVCM) based on level shifter approach was proposed that required a low bias voltage of order of ± 1.0V. In this technique, MOSFETs are either operating in saturation or in sub-threshold region. This circuit suffers the major drawback that flow of the offset current into the output transistor for the zero input current. Also with the increase in the number of transistors the power dissipation will also increase. However the major advantage offered by level shifting approach is the higher bandwidth at low voltages. The input resistance is also low, which is desirable for current mode circuits.

5. Proposed Current Mirror

The proposed current mirror shown in Fig.4 incorporates the advantage of cascode structure and level shifting approach. The cascade structure offers high output impedance and reduction of miller capacitance whereas level shifter approach offers low voltage requirements.

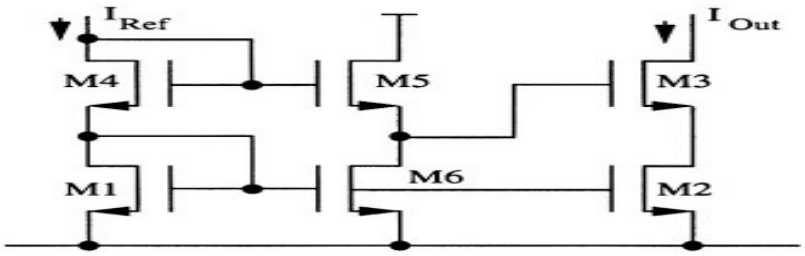

Figure 4: Proposed Level Shifted Casode Current mirror

The proposed structure M4 is shifting up the gate voltage of M1 and M5 is shifting down and M6 is used to control the current in the shifting down element. The reference current flows into M4. The overdrive of M5 is controlled by the current in M6 which mirrors the reference current. Therefore, the level shifting is controlled by transistor size ratios and bias currents and is independent of the threshold of n-channel elements. The proposed Current mirror is simulated for M4, M5and M3 having W=20 µm, L=0.15 µm whereas M1, M6 and M2 having W=1.4 µm, L=0.15 µm, the threshold voltage VTO=0.6 Volts, the bias current is taken 4mA for DC analysis. For simulation the supply voltage 2.0 volt is taken.

6. Simulation Results

The transfer characteristic is shown in figure 5. This result shows that the output current varies linearly with input current which confirms the current mirror copying the accurate current as the input current. So, the performance of the proposed circuit is better. Figure 6 and figure 7 shows the transient response of the proposed current mirror. For transient response analysis a pulse signal has been taken. This result shows that the output has settled after some delay; this is the settling time of the current mirror. The transition at output terminal is almost similar to input terminals with delay. The delay is due to the switching time of MOSFETs from one state to another state. Since the shuttling time of the proposed circuit is small, so its speed is also high and can be used in high speed CMOS applications.

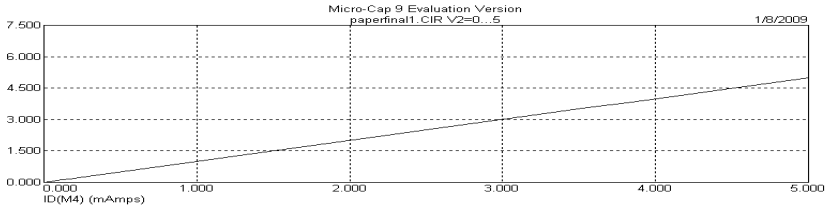

Figure 5: Variation of output Current with Input Current

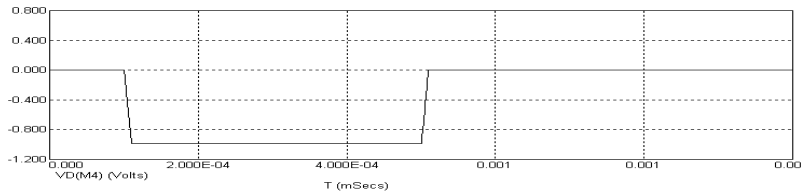

Figure 6: Variation of input Current with Input Current

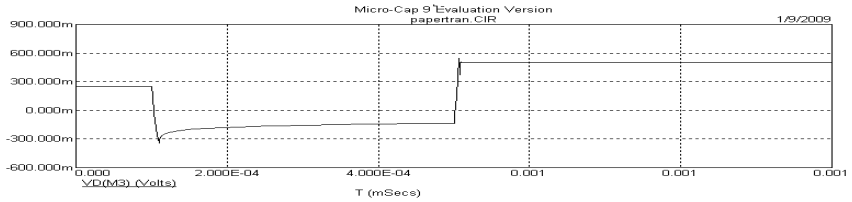

Figure 7: Variation of output Current with Input Current

7. Conclusion

Proposed high performance low voltage level shifted cascode current mirroring technique provides wide input and output range and high current transfer accuracy within a wide voltage range. Its shuttling time is small so its speed and thus performance has been increased. Therefore it is suitable for use in low voltage precision current-mode circuit design. In proposed low voltage and high performance current mirror the cascading approach increases the output impedance and level shifting approach reduces the power consumption.

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