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Small Signal Amplifier with P-Type Sziklai Pair

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Abstract: Significant modification is done in PNP Sziklai pair based small signal amplifier by modeling of paired device and deletion of a prominent biasing resistor from the circuit. This culminates into two discrete amplifier designs, proposed for the present studies. Both the proposed amplifiers simultaneously produce high voltage and current gain. However, bandwidth of one of the proposed amplifiers is found wider (195.603KHz) with higher THD whereas it is narrower (2.747KHz) for the other amplifier with lower THD. Qualitative behavior of proposed amplifiers is also analyzed on various scales like temperature dependency, noise dependency, impact of various biasing parameters on amplifier performance etc. The proposed amplifiers are found suitable to use in that kind of receiver/transmitter circuits where the band requirement limits between 2KHz to 195KHz.
Keywords: Sziklai pair, Small signal amplifier, Circuit Simulation, Analog communication.

1. Introduction

In recent years, Electronic Industry frequently uses Sziklai pairs in push-pull or quasi-complementary-symmetry power amplifier circuits[1,2]. However, Sziklai pair, as an alternative to Darlington pair, due to its half base turn ON voltage, better switching speed and better linearity, attracts much attention of the researchers at global level to explore its use in development of small signal amplifiers[1,3,4,5]. In recent years, Shukla et. al.[3] have been continuously involved to explore the applicability of Sziklai pair topology in small-signal amplifiers configured with different combinations of BJTs, JFETs and MOSFETs[4,6,7].

Similar to Darlington pair, Sziklai pair also comprises of two BJTs but of opposite polarity[1,2]. Unlike Darlington pair, collector of the first BJT in

Sziklai pair directly connects to the base of second. However, the current gain factor of Sziklai pair $\left(\beta_{\mathrm{szk}} = \beta_{Q_1}\beta_{Q_2} + \beta_{Q_1}\right)$ is slightly less than Darlington pair $\left(\beta_{\mathrm{dar}} = \beta_{Q_1}\beta_{Q_2} + \beta_{Q_1} + \beta_{Q_2}\right)$ due to small amount of in-built negative feedback but for higher β values current gain factor of both the devices are treated identical1,[2,3,5].

The present investigation is centered around the qualitative analysis of two P-type Sziklai pair based small signal amplifier circuits. Amplifiers under discussion are obtained by modifying the circuit of Shukla et. al.[3] which is referred herein as Reference Amplifier (Circuit-1). Proposed modification majorly accommodates modeling of Sziklai pair unit to receive superior outcomes along with removal of various consequences of Circuit-1.

2. Circuit Description

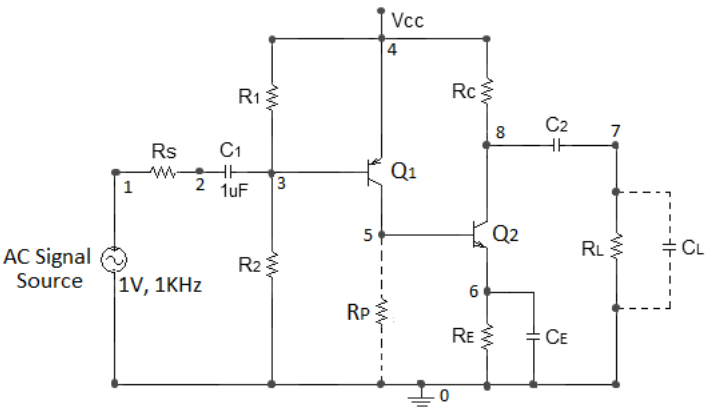

Figure 1. Describing basic circuit configuration of the amplifiers under discussion

Present investigation is done with the help of PSpice simulation[8]. The basic circuit idea to describe reference amplifier (Circuit-1) and both the proposed amplifiers (Circuit-2 and Circuit-3) is depicted in Fig.1. Circuit configuration of proposed amplifiers (Circuit-2 and Circuit-3) do not use additional biasing resistance RP as was an essential biasing component for the reference amplifier[3]. Rest of the circuit composition for present investigation is identical to what was used by Shukla et al[3] except the PNP-type Sziklai pair unit which uses PSpice default model in Circuit-2 and user defined model in Circuit-3. However, the proposed circuits are discussed in the present investigation both with and without the presence of RP and this is why the basic circuit configuration depicted in Fig.1 shows RP with dotted lines.

In the present investigation, the Sziklai unit of Circuit-2 uses PSpice default models of PNP and NPN type BJTs as Qbreakp ($\beta = 100$) and Qbreakn ($\beta = 100$) respectively whereas Circuit-3 uses user defined models of PNP and NPN type BJTs as QP ($\beta = 100$) and QN ($\beta = 50$) respectively[8].

Proposed amplifier circuits use voltage divider biasing network with +18V DC biasing source. Respective circuits are driven by 1V, 1KHz AC input signal to study amplification property. The qualitative analysis of Circuit-2 amplifier is observed for 10mV, 1KHz input signal whereas this for Circuit-3 is done for 1mV, 1KHz. However, Circuit-2 produce faithful amplification of input AC signal in .001mV to 40mV range whereas this range for Circuit-3 amplifier is .0001mV to 8mV.

Table 1 Component Details of the Circuits Under Discussion

Component Details	Circuit-1 (Reference Amp)	Circuit-2 (Proposed Amp)	Circuit-3 (Proposed Amp)
Q_1 (PNP BJT)	Q2N2907A	Qbreakp	QP
Q_2 (NPN BJT)	Q2N2222	Qbreakn	QN
R_S	500Ω	100Ω	100Ω
R_1	33KΩ	33KΩ	33KΩ
R_2	100KΩ	100KΩ	100KΩ
R_C	10KΩ	10KΩ	10KΩ
R_E	2KΩ	1KΩ	1KΩ
R_L	10KΩ	10KΩ	10KΩ
R_P	500Ω	-	-
C_1 and C_2	1μF	.1μF	1μF
C_E	0.1μF	0.001 μF	0.1 μF
VCC	+18V DC	+18V	+18V
AC Signal	1V, 1KHz	1V, 1KHz	1V, 1KHz
AC Signal range	10-30mV	0.001-40mV	0.0001-8mv

Active and passive parameters describing reference amplifier (Circuit-1) and both the proposed circuits (Circuit-2 and Circuit-3) under discussion are mentioned in Table-1 whereas Table-2 describes a close comparison of the simulation parameters for commercial BJTs used in reference amplifier and the BJT Spice models of Sziklai pairs in the proposed amplifier circuits.

Refer Table-2. The PNP type BJT in Reference Circuit-1 (Q2N2907A) operates with current amplification factor $\beta = 231.7$ whereas this for PNP type BJT models in proposed Circuit-2 (Qbreakp) and Circuit-3 (QP) is chosen as $\beta = 100$. Similarly, β for NPN type BJT in Reference Circuit-1

(Q2N2222) is kept 255.9 by the manufacturer whereas this for similar kind of BJTs in Circuit-2 (Qbreakn) and Circuit-3 (QN) is modeled to be 100 and 50 respectively8. Table-II also describes that which simulation parameter for respective BJTs are chosen with default values and which are defined by either manufacturer (Circuit-1), PSpice software (Circuit-2) or by the user (Circut-3).

Table 2 Simulation Parameters For Commercial and Modeled BJTs

Parameter Description	BJT Models With Respective Parameter Values					
	Q2N2907A (PNP)	Q2N2222 (NPN)	Qbreakp (PNP)	Qbreakn (NPN)	QP (PNP)	QN (NPN)
IS	650.6E-18	14.34E-15	100E-18	100E-18	200E-18	200E-18
BF	231.7	255.9	100	100	100	50
NF	1	1	1	1	1	1
VAF	115.7	74.03	Default	Default	1	1
ISE	Default	Default	Default	Default	54.8E-15	14.34E-15
NE	1.829	1.307	Default	Default	Default	Default
BR	3.563	6.092	1	1	Default	Default
NR	1	1	1	1	Default	Default
RB	10	10	Default	Default	5	5
RC	0.715	1	Default	Default	1	1
RE	Default	Default	Default	Default	0	0
CJE	19.8E-12	22.01E-12	Default	Default	400E-15	-
VJE	Default	Default	Default	Default	0.8	-
MJE	0.3357	0.377	Default	Default	0.4	-
CJC	14.7E-12	7.306E-12	Default	Default	500E-15	Default
MJC	.5383	.3416	Default	Default	Default	Default
VJC	Default	Default	Default	Default	0.8	Default
CJS	Default	Default	Default	Default	1.0E-12	Default
TF	603.7E-12	411.1E-12	Default	Default	200E-12	200E-12
XTF	1.7	3	Default	Default	Default	Default
VTF	5	1.7	Default	Default	Default	Default
ITF	0.65	0.6	Default	Default	Default	Default
TR	111.3E-09	46.91E-09	Default	Default	5.0E-09	5.0E-09

3. Results and Discussions

Variation of voltage gain with frequency of the proposed amplifiers is depicted in Fig.2 whereas various performance parameters are recorded in Table-3. Fig.2 clearly indicates that proposed amplifiers with Sziklai pair are free from the poor response problem of small signal Darlington pair amplifier at higher frequencies[9,10].

Table 3 Performance Parameters At Room Temperature 27OC

Performance Parameters	Circuit 1 (Reference Amplifier)	Circuit 2 (Proposed Amplifier)	Circuit 3 (Proposed Amplifier)
Maximum Voltage Gain A_{VG}	102.309	290.971	209.266
Maximum Current Gain A_{IG}	7.3458	8.265	7.3865
Upper Cut Off Frequency f_H	5.0153 KHz	201.133 KHz	3.141 KHz
Lower Cut Off Frequency f_L	210.108 Hz	5.530 KHz	393.895 Hz
Band-Width B_W	4.80 KHz	195.603KHz	2.747 KHz
Maximum Output Current I_O	110.6μA	50.905 μA	22.064 μA
Maximum Input Current IS	13.502 μA	6.2491 μA	3.0688 μA
Maximum Output Voltage V_O	1.106V	504.347 V	220.575
Maximum Input Voltage V_S	9.859mV	9.991 mV	0.9989mV
Output Phase Difference θ^O	180^O	180^O	180^O
Total Harmonic Distortion THD	1.72%	2.154%	1.015%

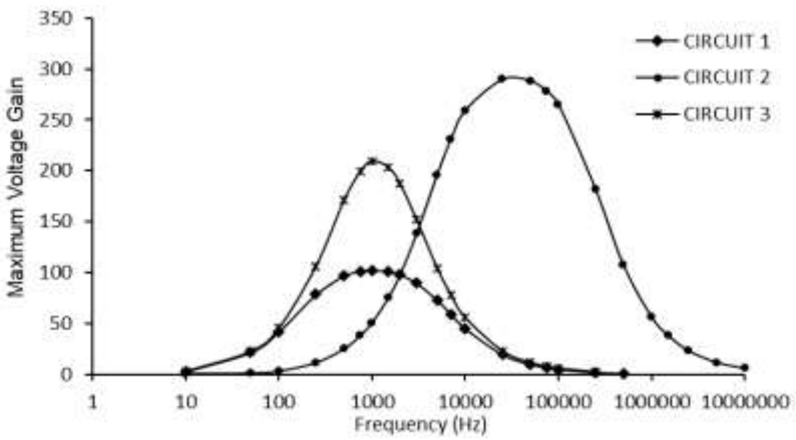

Figure 2. Variation of Voltage gain with frequency for reference and proposed amplifiers

Records in Table-3 and the graph of Fig.2 suggests that Circuit-2 provides faithful amplification in 5.530KHz to 201.133KHz range of frequency with 290.971 maximum voltage gain (AVG). However, Circuit-3 is capable of producing faithful amplification in 393.895Hz to 3.141KHz range of frequency with 209.266 maximum voltage gain. Thus, modeling of Sziklai pair in Circuit-2 reveals response range of the amplifier to moves around higher frequency region for faithful amplification with wider bandwidth and almost 284% higher voltage gain than reference amplifier whereas Circuit-3 reveals a response range close to the reference amplifier circuit with narrower bandwidth and almost 204% higher voltage gain than reference amplifier. In addition, the increase in current gain is also observed for Circuit-2 whereas current gain for Circuit-3 is found almost identical to the Circuit-1. Similarly, THD for Circuit-2 is reported to be minorly higher but for Circuit-3 it is lower than THD of the reference amplifier circuit.

It is interesting to note that when β is kept 150 in user defined model of PNP BJT of Ciruit-3 (keeping $\beta = 50$ in NPN BJT model), the voltage gain AVG drops to 6.7224 (with 10KHz mid frequency), current gain AIG drops to 0.745, lower cut off frequency fL and upper cut off frequency fH raised to reach at 1.408KHz and 68.243KHz respectively (Bandwidth BW=66.835KHz) with significant enhancement in THD which climbs to 4.486%. Therefore, varying β of PNP BJT of Circuit-3 between 50 to 150 may widen the bandwidth on the cost of reduced voltage gain. Contrarily, when β is kept 150 in User defined model of NPN BJT of Ciruit-3 (keeping $\beta = 100$ in PNP BJT model), voltage gain (AVG=209.265) and current gain (AIG=7.3864) drops to a nonsignificant value with no change in THD. This suggests the importance of driver BJT in the circuit model of Sziklai pair (PNP in present case) which draw significant influence on the amplifier performance.

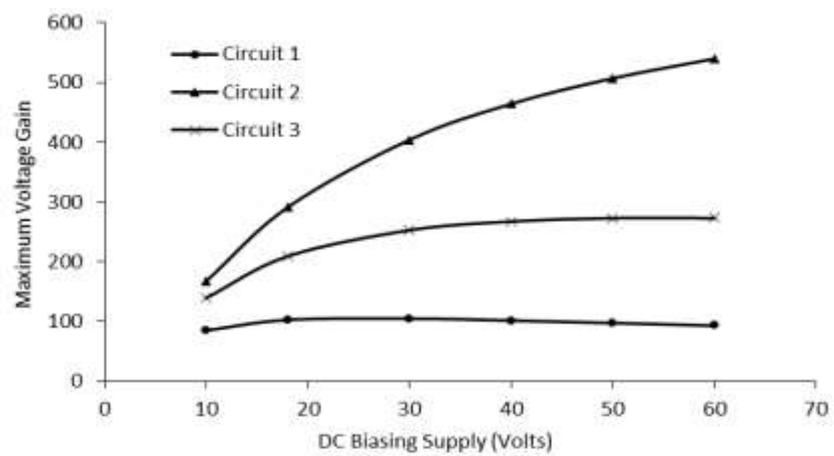

Figure 3. Variation of voltage gain with DC biasing supply

Variation of voltage gain with DC biasing voltage is depicted in Fig.3. It is observed here that Sziklai pair in all the three amplifiers under discussion switches ON at 10V and the respective amplifiers provide faithful amplification in 10-60V range of DC biasing voltage. The basic difference between the three amplifiers under investigation is that the voltage gain raised to maximum for Circuit-1 amplifier at 30V and thereafter it starts decreasing with increasing biasing voltage. However, for Circuit-2 and Circuit-3 amplifiers the voltage gain climbs to a maximum at 60V and 50V respectively. The curve depicting the variation of voltage gain with respect to DC biasing voltage attains almost saturation beyond 50V for Circuit-3 amplifier whereas it has a gradual rising tendency for Circuit-2.

It is also interesting to observe the qualitative behaviour of proposed amplifiers (Circuit-2 and Circuit-3) under three different situations. First on removal of biasing resistance RS (Condition A), second with inclusion of additional biasing resistance RP (Condition B), and third with inclusion of RP and removal of RS (Condition C) simultaneously. The observed qualitative parameters under these situations are summarized in Table-4.
Records in Table-4 revels that the situation which includes RP in respective circuits is responsible for significant enhancement in bandwidth but on the cost of considerable declination in voltage and current gains. Status of fL under this situation indicates the shifting of response curve towards higher frequencies with the only exception for Circuit-2 under Condition-C.

Table 4 Performance Parameters of Proposed Circuits Under Different Situations

Parameter	Circuit-2			Circuit-3		
	Condition A	Condition B	Condition C	Condition A	Condition B	Condition C
A_{VG}	468.105	110.478	174.972	290.996	104.910	154.793
A_{IG}	8.272	3.0822	3.083	7.3864	3.2511	3.251
f_H (KHz)	191.129	513.856	507.941	3.535	6.309	6.832
f_L (Hz)	905.646	5.678	904.904	527.326	484.427	679.016
B_W (KHz)	190.223	508.178	507.036	3.007	5.824	6.152
THD	9.179%	1.755%	6.457%	1.478%	1.526%	1.707%

Similarly, removal of RS from Circuit-2 records significant enhancement in AVG and THD with almost unaltered AIG and small amount of reduction in bandwidth. However, this with Circuit-3 gives considerable improvement in AVG and bandwidth along with a minor enhancement in THD. Removal of RS from Circuit-3 brings its qualitative behaviour near to the reference Circuit-1 with advantage of minor enhancement in AVG on the cost of minor reduction in bandwidth and THD. Thus Circuit-2 and Circuit-3 under Condition-A may be favourable choice for different applications of electronic communication.

Observed variations in performance parameters with respect to temperature are comprised in Tables-5 and 6. It is clear by respective tables that the voltage gain, bandwidth and THD are decreasing with the rise of temperature for both the proposed amplifiers. Observation reveals that both the proposed amplifiers (Circuit-2 and Circuit-3) perform better at lower temperature. This declination in voltage gain is perhaps due to rise of collector-base leakage current of second BJT with rising temperature which in-turn elevates the collector current and caused lowering of output voltage[3,10].

Table 5 Variation of Performance Parameters with Temperature for Circuit-2

Temp. (^{O}C)	A_{VG}	A_{IG}	F_L (KHz)	F_H (KHz)	B_W (KHz)	THD (%)
-30	326.432	8.276	6.180	203.782	197.602	2.148
-20	319.500	8.274	6.017	202.737	196.720	2.149
-10	312.895	8.272	5.858	202.484	196.626	2.150
0	306.597	8.270	5.796	201.986	196.190	2.151
10	300.583	8.268	5.652	201.820	196.168	2.152
20	294.838	8.267	5.544	201.648	196.104	2.153
27	290.971	8.265	5.530	201.133	195.603	2.154
50	279.060	8.261	5.294	200.869	195.575	2.155

Table 6 Variation of Performance Parameters with Temperature for Circuit-3

Temp. (^{O}C)	A_{VG}	A_{IG}	F_L (Hz)	F_H (KHz)	B_W (KHz)	THD (%)
-30	230.064	7.418	426.924	3.218	2.791	1.135
-20	225.987	7.413	419.260	3.199	2.779	1.118
-10	222.105	7.407	411.878	3.182	2.770	1.082
0	218.319	7.401	408.166	3.167	2.758	1.067
10	214.673	7.396	399.377	3.153	2.753	1.051
20	211.457	7.390	394.204	3.143	2.749	1.026
27	209.266	7.386	393.895	3.141	2.747	1.015
50	202.391	7.373	388.283	3.083	2.694	0.951

Table 7 Variation of Input Noise and Output Noise with Temperature

Temperature (^{O}C)	Output/Input Noise for Circuit 2 (at 1KHz)		Output/Input Noise for Circuit 3 (at 1KHz)	
	OUT NOISE (V/Hz) x 10-7	IN NOISE (V/Hz) x 10-8	OUT NOISE (V/Hz) x 10-7	IN NOISE (V/Hz) x 10-9
-30	5.594	1.099	4.056	1.774
-20	5.601	1.101	4.033	1.793
-10	5.608	1.104	4.010	1.811
0	5.615	1.106	3.987	1.829
10	5.622	1.108	3.965	1.847
27	5.633	1.112	3.928	1.877
50	5.649	1.117	3.880	1.917

On the other hand, Input and Output noises for proposed amplifiers at operating frequency (1KHz) is observed at different temperatures and listed in Table-7. Normally, active and passive components of the circuit are responsible to generate noise during the circuit operation[6]. In the present case of proposed amplifiers, respective noises at defined frequencies are found low enough and within the permissible limit.

It is also observed for Circuit-2 that Input and Output noises at 1KHz operating frequency increases with the temperature elevation. However, for Circuit-3, Input noise increases whereas Output noise at 1KHz decreases with temperature elevation.

Biasing resistances always play important role in amplifier performance. Tables 8, 9, 10A and 10B show performance of Circuit-2 and Circuit-3 respectively at minimum (MIN) and maximum (MAX) possible values of the biasing resistances R_1, R_2, R_E, R_C and R_L for faithful amplification. Respective observations are taken by varying one resistance at a time keeping others constant.

Table 8 Performance of Circuit-2 at Min. and Max. Values of R_1, R_2 and R_E

Performance Parameters	R_1		R_2		R_E	
	5KΩ MIN	90KΩ MAX	40KΩ MIN	400KΩ MAX	50Ω MIN	1.5KΩ MAX
A_{VG}	44.647	310.478	1.038	56.397	17.745	7.061
A_{IG}	6.088	8.297	0.107	7.933	0.409	0.749
B_W (KHz)	191.821	197.593	28521.59	191.83	3219.23	5715.99
f_H (KHz)	193.012	203.453	28537	192.978	3225	5731
f_L (KHz)	1.191	5.806	15.409	1.148	5.767	15.003
THD (%)	4.646	3.090	3.214	4.592	2.141	5.619

Table 9 Performance of Circuit-3 at Min. and Max. Values of R_1, R_2 and R_E

Performance Parameters	R_1		R_2		R_E	
	5KΩ MIN	110KΩ MAX	100KΩ MIN	470KΩ MAX	30Ω MIN	1KΩ MAX
A_{VG}	54.814	216.149	209.266	43.851	11.994	209.266
A_{IG}	7.021	7.220	7.386	8.660	0.339	7.386
B_W (KHz)	2.067	2.795	2.747	2.006	54.025	2.747
f_H (KHz)	2.186	3.207	3.141	2.086	54.608	3.141
f_L (Hz)	118.638	411.039	393.895	79.415	582.249	393.895
THD (%)	0.517	1.047	1.015	0.567	1.613	1.015

Refer observations for Circuit-2 in Table-8. If RE is varied above and below its defined value 1KΩ, the voltage gain reduces significantly, lower cut-off frequency reaches below 16KHz and the bandwidth extends to MHz range. This shows the viability of amplifier to amplify 5KHz-5.73MHz range frequency signals, if R_E is controlled properly. Contrarily, Circuit-3 does not produce faithful amplification beyond 1KΩ value of R_E but on minimum possible value of R_E, this amplifier presents a wider bandwidth on the cost of significantly reduced voltage and current gains.

Table 10A Performance of Circuit-2 at Min. and Max. Values of R_C and R_L

Performance Parameters	R_C		R_L	
	660Ω MIN	500KΩ MAX	500Ω MIN	400KΩ MAX
A_{VG}	135.639	316.095	114.169	315.864
A_{IG}	3.792	9.001	63.608	0.225
B_W (KHz)	421.396	183.65	502.845	180.351
f_H (KHz)	427.033	189.088	508.727	185.915
f_L (Hz)	5.637	5.438	5.882	5.546
THD (%)	2.507	2.155	1.298	2.197

Table 10B Performance of Circuit-3 at Min. and Max. Values of R_C and R_L

Performance Parameters	R_C		R_L	
	700Ω MIN	250KΩ MAX	100Ω MIN	290Ω MAX
A_{VG}	116.131	222.732	28.538	222.419
A_{IG}	3.673	7.969	81.701	0.276
B_W (KHz)	4.815	2.558	19.568	2.556
f_H (KHz)	5.274	2.945	20.148	2.945
f_L (Hz)	458.724	386.845	579.364	388.251
THD (%)	1.349	0.962	1.911	0.907

Voltage gain of both the amplifiers significantly improves on higher values of R_C and R_L but beyond the maximum permissible values of respective resistances, respective voltage gains acquire a tendency of saturation. Similarly, at lower R_L values, current gain and bandwidth of both the amplifiers improves drastically on the cost of reduced voltage gain.

Lowering the value of R_1 in both the amplifiers reduces voltage gain, bandwidth and the current gain whereas its rising value gives the enhanced voltage gain and bandwidth with a minor variation in current gain. On the other hand, increasing R_2 in Circuit-2 causes reduction in voltage gain and elevation of THD but at minimum value of R_2, Voltage gain reaches almost near to unity with current gain below unity but drastically improved bandwidth which expands to reach in MHz frequency range. Contrarily, increasing R_2 in Circuit-3 causes reduction in voltage gain, bandwidth and THD on the cost of improved current gain.

Table 11 Performance of Circuit-2 at Different Values of C_E in Absence of C_L

Capacitance	A_{VG}	A_{IG}	F_L (KHz)	F_H (KHz)	B_W (KHz)	THD (%)
1.00 pF	299.848	8.272	5.861	187290	187284	1.77
0.01 nF	299.766	8.272	5.805	18895	18889	1.78
0.10 nF	298.948	8.272	5.820	1942	1936	1.77
1.00 nF	290.971	8.262	5.487	200.621	195.134	2.15
0.01 μF	229.952	8.203	3.891	28.751	24.860	2.18
0.10 μF	74.288	7.633	1.253	8.707	7.454	2.21
1.00 μF	9.4979	4.502	0.2658	6.237	5.971	1.06

Table 12 Performance of Circuit-2 at Different Values of C_L Keeping C_E Fixed

Capacitance	A_{VG}	A_{IG}	F_L (KHz)	F_H (KHz)	B_W (KHz)	THD (%)
1.00 pF	290.961	8.265	5.526	201.102	195.576	2.472
0.01 nF	290.869	8.265	5.462	200.444	194.982	2.437
0.10 nF	289.923	8.258	5.509	181.857	176.348	1.883
1.00 nF	280.315	8.190	5.298	106.704	101.406	0.836
0.01 μF	211.025	7.572	3.787	28.279	24.492	0.281
0.10 μF	60.132	4.313	1.773	11.219	9.446	0.982
1.00 μF	7.3705	0.813	1.231	8.684	7.453	1.302

Performance parameters for both the proposed circuits are observed at different values of Emitter By pass Capacitor C_E and Load Capacitor C_L. Respective records are listed in Tables 11, 12, 13 and 14. Observations corresponding to variation in C_E is taken in absence of C_L whereas performance parameters corresponding to variation in C_L are observed by keeping C_E unchanged.

Table 13 Performance of Circuit-3 at Different Values of C_E in Absence of C_L

Capacitance	A_{VG}	A_{IG}	F_L (Hz)	F_H (KHz)	B_W (KHz)	THD (%)
1.00 pF	265.761	7.442	577.390	8608	8607.4	1.74
0.01 nF	265.757	7.442	570.565	6816	6815.429	1.74
0.10 nF	265.697	7.442	570.008	1824	1823.429	1.73
1.00 nF	265.052	7.442	567.361	211.658	211.091	1.72
0.01 μF	258.760	7.436	541.576	22.481	21.939	1.69
0.10 μF	209.266	7.386	390.768	3.1365	2.988	1.02
1.00 μF	72.278	6.917	133.776	0.9263	0.7925	1.57

It is clear by the observations in Tables 11 and 13 that decreasing value of C_E in both the proposed amplifiers cause elevation in voltage gain, current gain and THD along with widening of the bandwidth. Bandwidth at

lowest value of C_E (1pF) for Circuit-2 provides a vast range of frequency for faithful amplification, extended from 5.861KHz to 187.290MHz. However, for Circuit-3 at 1pF of CE, the faithful amplification range extends from 577.390Hz to 8.608MHz frequency. This feature meets out the need of a high-voltage-gain-wide-band audio amplification of mV range AC signals.
It can be also be stated on the basis of observations recorded in Tables 8, 9, 10, 11, 12, 13 and 14 that the appropriate combination of R_E-C_E or R_L-C_L or C_E-C_L for both the proposed amplifiers may lead a facility of simultaneous adjustment of the gain and bandwidth as per the need of communication circuits like transmitter/receiver.

Table 14 Performance of Circuit-3 at Different Values of C_L Keeping C_E Fixed

Capacitance	A_{VG}	A_{IG}	F_L (Hz)	F_H (KHz)	B_W (KHz)	THD (%)
1.00 pF	209.265	7.386	394.031	3.120	2.726	1.015
0.01 nF	209.260	7.386	391.786	3.119	2.726	0.662
0.10 nF	209.210	7.385	395.170	3.118	2.723	0.235
1.00 nF	208.708	7.379	391.219	3.095	2.704	0.282
0.01 µF	203.684	7.320	383.115	2.903	2.519	0.269
0.10 µF	161.663	6.766	316.442	1.994	1.677	0.222
1.00 µF	52.138	3.850	176.437	1.089	0.912	0.534

Small-signal AC equivalent circuit corresponding to proposed amplifiers is depicted in Fig.4(a) whereas values of various small signal AC parameters corresponding to BJTs used in Sziklai pairs in all the three circuits are listed in TABLA-15.

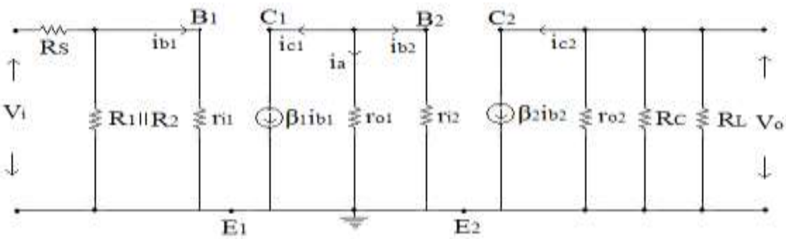

Figure 4(a). Small signal AC equivalent circuit corresponding to proposed amplifiers

Since $R_1 \| R_2$ ($\approx$ 24.81KΩ) is much higher than R_S ($\approx$ 100Ω) and ro2, R_C, R_L are in parallel, therefore the equivalent circuit of Fig.4(a) can be reduced to as depicted in Fig.4(b).

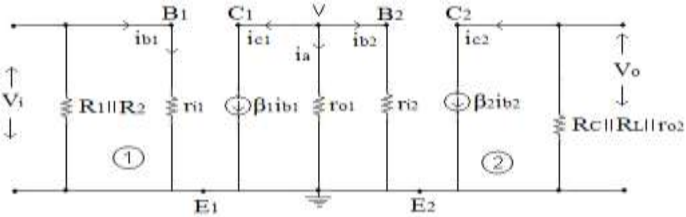

Figure 4(b). Reduced AC equivalent circuit corresponding to the proposed amplifiers

Analysis of Fig.4(b) suggests following expression for the AC voltage gain of the proposed amplifiers

$$A_V = \frac{-\beta_1\beta_2\left(R_C \parallel R_L \parallel r_{O_2}\right)}{r_{i1}\left[1+\dfrac{r_{i2}}{r_{O_1}}\right]}.$$

Similarly the expression for the AC current gain of the circuits under consideration may be given as

$$A_I = \frac{-\beta_1\beta_2}{\left[1+\dfrac{r_{i1}}{R}\right]\left[1+\dfrac{r_{i2}}{r_{O_1}}\right]}$$

Table 15 Small Signal AC Parameters for Modelled BJTs in Sziklai Pairs

Small Signal AC Parameter for BJTs	Device Model (Circuit-1)		Device Model (Circuit-2)		Device Model (Circuit-3)	
	Q2N2907A PNP	Q2N2222 NPN	Qbreakp PNP	Qbreakn NPN	QP PNP	QN NPN
IB	-0.000147	0.006	-0.00015	1.46E-02	0.00015	0.0148
IC	-0.0336	4.99E-04	-1.46E-02	3.07E-04	-0.0148	0.000286
VBE	-0.818	0.803	-8.44E-01	0.861	-0.826	9.17E-01
VBC	3.37	0.797	1.39E+00	8.43E-01	1.14	8.99E-01
VCE	-4.19	5.30E-03	-2.23E+00	1.82E-02	-1.96	1.85E-02
BETA DC	200.29	0.0831	100	211	101	193
GM	1.26	0.218	0.565	5.65E-01	5.73E-01	5.62E-01
RPI	177	127	177	89.40	176	44.90
RX	10.0	10.00	0.00	0.00	5.00	5.00
RO	3540	0.838	1.00E+12	1.81	6820	1.81
CBE	8.03E-10	5.97E-10	0.00	0.00	1.15E-10	2.23E-10
CBC	5.92E-12	6.40E-08	0.00	0.00	3.74E-13	2.76E-09
CJS	0.00	0.00	0.00	0.00	1.00E-12	0.00
BETA AC	223	27.60	100	50.50	101	25.20

4. Conclusions

Two circuits of PNP Sziklai pair based small signal amplifiers, with different qualitative properties, are designed by modeling of paired device and deletion of additional biasing resistance R_P. Proposed amplifiers may be used in that kind of receiver/transmitter type of communication circuits where the band requirement limits between 2KHz to 195KHz. Qualitative performance of both the proposed amplifiers are examined with respect to variations in various biasing resistors and capacitors. Respective amplifiers are found to produce faithful amplification in -30oC to 50oC temperature range with low order input and output noises and 10V-60V permissible DC biasing voltage range.

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