

On Low Power CMOS Operational Transconductance Amplifier Structures

Geetika Srivastava, Aditya K. Sharma and Sachchidanand Shukla

Department of Physics and Electronics
Dr. Rammanohar Lohia Avadh University, Ayodhya-224001
Email-geetika_gkp@rediffmail.com

Ashish Dixit and Anil Kumar

Department of Electronics
Amity University Uttar Pradesh, Lucknow- 226001

(Received June 16, 2019)

Abstract: Emerging field of System on Chip(SoC) design require powerful on chip mixed signal processing capability that require powerful analog signal processing block along with the logic processing digital block. These powerful analog IC design capabilities are also required in many battery operated, low power-low frequency applications The growing demand of low power, portable and biomedical devices require low power low noise analog ICs. These analog ICs use Operational Transconductance Amplifiers or OTA as they are generally called, as their main component. OTAs are special type of Operational Amplifiers that have additional capability of tune able gain along with higher output impedance. The OTAs are used as basic building blocks in Analog IC designing. In this article, four different OTA structures are reviewed with high DC gain, high speed, linearity and design flexibility. We have reviewed architecture of power optimized OTA's with respect to their usability as active filters, as programmable CMOS-OTA, and analog and mixed analog-digital signal processing systems.

Keywords: Transconductance Amplifier, OTA, Analog CMOS IC Design, Low Power VLSI, SoC Design

1. Introduction

OTAs are a type of amplifier that outputs current based on differential input voltage applied. Many authors used OTA as an active element in their circuits, essentially a voltage-controlled current source (VCCS) with main

design parameter g_m , the transconductance g_m . OTA is an important block in analog design as it is capable of implementing almost any analog components including amplifier, current conveyer, filter to name a few and for these analog circuits the OTAs are required to have high- performance characteristics, such as low power consumption and a fast settling response. The most desirable is a settling behaviour that is limited by the non-slew rate. Its transconductance g_m can be used as a design parameter as it can be varied or programmed by an external controlling current or voltage. This programmability of g_m gives circuit designer a freedom to manipulate many design parameters. Unlike OpAmps the OTAs do not require equal voltage to be applied on both its inputs hence a differential voltage swing is possible in OTAs.

In recent years, many advances have been reported in improvement of linearity of MOS transconductor circuit¹. Several good linearity CMOS Operational Transconductance Amplifier (OTA) structures have been successfully implemented for high-frequency filter applications and the parameters of this circuit have been improved as per desirable applications². OTAs are very important devices that convert an input voltage to an output current with a constant transconductance with infinite input and output impedances. The OTAs are mainly voltage to current amplifiers. This takes the difference between the two input voltages for conversion into output current.

2. Basic Configuration of OTA

Based on input and output configurations, OTAs can be divided into three types: single input/output, differential-input single-output, and differential input/output (fully differential). The other possible type, single-input differential-output, is not practical and it has not been used in another application.

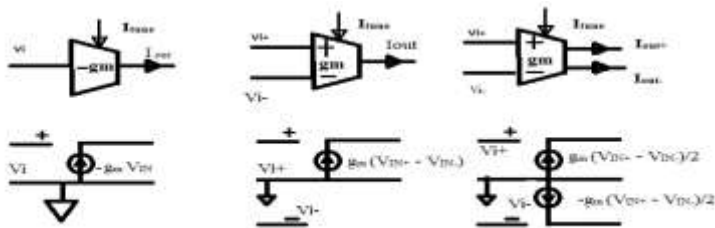


Figure 1. Three types of OTAs and their equivalent circuit models: (a) Single-Input / Output, (b) Differential-Input Single-Output, and (c) Differential Input / Output

The output currents of these three types of OTAs Fig. 1(a), 1(b), 1(c) respectively are

$$(2.1) \quad 1, \text{ for 1(a),}$$

$$(2.2) \quad I_{out} = g_m (V_{IN+} - V_{IN-}), \text{ for 1(b) and}$$

$$(2.3) \quad I_{out} = I_{out+} - I_{out-} = g_m (V_{I0} - V_{I0}) \text{ or 1(c).}$$

With these three types of OTAs, the transconductance g_m can be set via their DC current bias I_{tune} . The single input/output transconductor shown in Fig. 1-1(a) is the easiest to implement, e.g. a single NMOS trans conductor with a common source. The simplicity of this type of OTA makes it attractive in complex implementation. The differential configurations in Fig. 1(b) and Fig. 1(c) are preferred due to their common-mode rejection and their flexibility to activate feedback configurations³⁻⁶. The two differential types in Fig. 1(b) and 1(c) have almost the same performance and can be replaced by each other in most circuits using OTAs (Silva-Martinez). Adjusted structures utilizing differential input and differential output OTA's can accomplish exceptionally high common-mode rejection ratio (CMRR) and lessen both the even-order harmonic distortion segments and the impacts of the power supply noise⁷.

An ideal OTA consists of two voltage inputs with infinite impedance, as there are no input currents and the common-mode input range is ideally infinite. However, the differential signal between the two inputs is used to control output current and does not depend on the output voltage, as an ideal current source. The ideal transfer characteristics is described as

$$(2.4) \quad I_{out} = g_m (V_{IN+} - V_{IN-}),$$

Where transconductance g_m is constant in ideal condition.

The current CMOS integrated circuits are facing challenges in high frequency, linearity, and low power and so does the CMOS OTAs face these three major challenges. Many recent significant efforts have been done by some researchers and many latest publications have reported significant improvement in three parameters of CMOS OTA based circuits. Meanwhile, there are still challenges of trade-off between these parameters while designing realistic OTAs.

The bulk pushed CMOS is the common technique reported in many literatures that allow us operation in even lower operating voltages. The bulk voltage allows us to operate MOS in sub threshold region and gives the room of threshold voltage drop minimization. However this technique has its own drawbacks in terms of noise performance. OTA implemented through bulk pushed MOS has improved ultra-low voltage rail-to-rail operation characteristics.

3. Low Operating Voltage Bulk Driven MOS

OTAs as main analog building blocks face a bigger problem in CMOS implementation as the ever decreasing geometry of CMOS reduce the operating voltage swing and hence the threshold voltage drop in MOS transistors limits the operation of MOS based OTA⁸⁻¹⁰. Among the various popular schemes of low voltage MOS operation like level shifter technique, rial-to-rail input/output stages, the floating gate approach, self-cas code structures, and the bulk-driven (BD) technique, the sub threshold (weak inversion) region operation is the most suitable one in OTA design. This allows further power reduction in CMOS circuits as they are working in weak inversion region, also they are good choices since they have high g_m ratio. The bulk driven saturation drain current is given by¹¹

$$(3.1) \quad I_D = \frac{1}{2} k'_p \left(\frac{W}{L} \right) \left(V_{GS} - |V_{TH}| \right)^2,$$

where symbols have their usual meaning and the threshold voltage is given by

$$(3.2) \quad |V_{TH}| = |V_{TH0}| + |\gamma| \left[\sqrt{2|\phi_F + V_{BS}|} - \sqrt{2|\phi_F|} \right],$$

with $V_{BS} \neq 0$, the transconductance of bulk operated MOS is given by

$$(3.3) \quad g_{mb} = \frac{dI_D}{dV_{SB}} = \frac{|\gamma| g_m}{2\sqrt{2|\phi_F + V_{BS}|}} = \frac{|\gamma| \sqrt{2\beta I_D}}{2\sqrt{2|\phi_F + V_{BS}|}}.$$

The MOS drain current in weak inversion is given by

$$(3.4) \quad I_{DS} = I_s \left(\frac{W}{L} \right) \exp \left(q \frac{V_{GS} - V_{TH}}{nkT} \right) \left[1 - \exp \left(-q \frac{V_{DS}}{kT} \right) \right]$$

and the transconductance g_m is given by

$$(3.5) \quad g_m = q \frac{I_{DS}}{nkT}.$$

The change in transconductance due to bulk driving, is represented by η , which given as

$$(3.6) \quad \eta = \frac{g_{mb}}{g_m} = \frac{\gamma}{2\sqrt{2|\phi_F + V_{BS}|}},$$

where g_{mb} varies 20 to 50% of g_m ¹².

The noise performance of the bulk operated MOS decreases significantly. Another structure that uses current-shunt auxiliary differential pairs to improve the voltage gain from the inputs to the gates of the bulk-driven pairs results in enhanced transconductance. The enhanced transconductance leads to the improvement of gain bandwidth and dc gain of the OTA with a higher figure-of-merit (FoM)¹³.

4. A bulk-driven CMOS OTA with high DC Gain

The fully differential topology¹⁴ discusses the operation of 0.8-volt OTA where rail to rail swing is achieved by two input differential pairs, one implemented using PMOS and other using NMOS and driven by bulk. The amplifier core is based on a fully differential topology Fig.2 and input pairs are complementary common gate amplifiers using cas code current loads operations.

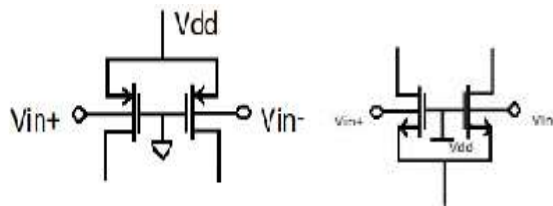


Figure 2. Bulk Operated NMOS and PMOS Differential Pairs

The input common-mode can be increases to its highest possible range in this configuration. As the input common-mode voltage is increased from low to high, and then there are three operating conditions of the differential pair. First when p-type differential pair is on and n-type differential pair is off, Second condition when p-type differential pair is off and n-type differential pair is on, and third when the input common-mode is in middle of the range then both pairs are on. These conditions result in rail to rail operation of the circuit.

In the output, there are two common gate amplifiers of symmetric type and for increasing gain the current loads used by amplifiers must be increased. The high value of open loop gain can be obtained through inclusion of several auxiliary common source amplifiers. Gate of common gate amplifier (CG) and output of the common source amplifier (CS) are connected to each other to maintain almost constant source voltage Fig.3.

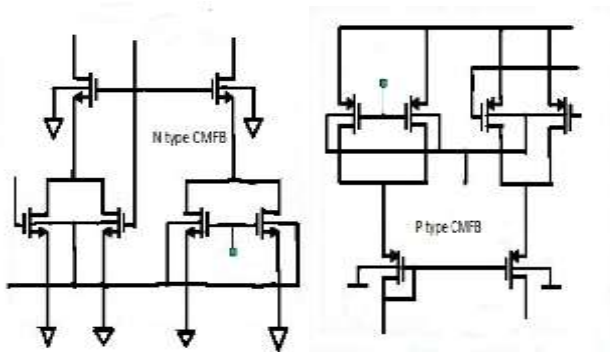


Figure 3. N and P type Common Mode Feedback (CMFB) blocks

Some transistors of this configuration operating in the linear region and if the DC operating point at the output deviates from the common mode target voltage, the final current of the input pair changes, resulting in an increase or decrease in the bias currents. The operation of transistors in the saturation region can be ensured by applying fixed bias voltage on the gate of transistors or on the body of transistors. Bias voltage is generated by simple voltage dividers and a low sensitivity reference current generator circuit Fig.4.

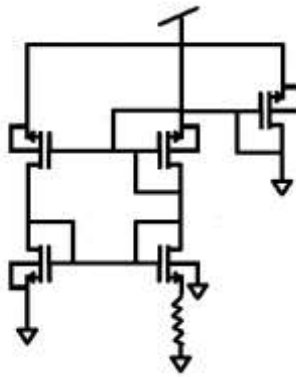


Figure 4. Reference Current generator

Performance evaluation of the OTA is done on two parameters phase response and gain. This open loop circuit has a gain of 68 dB, a unity-gain bandwidth of 93 MHz, and a phase margin of 80, there under no-load condition. The disadvantage of bulk-controlled lower transconductance, low-gain technology is overcome in this configuration by using amplifiers, allowing a high DC gain.

5. Gain-Boosted CMOS OTA with High-Speed Optimization

Paper¹⁵ is about OTA structure made by purposely putting complex conjugate poles in the general transfer function. This paper and also discusses the methodology to control the separation of these two poles. It guarantees there is no slow-settling part as the pole-zero doublets in the transient response. The ideal detachment between the complex poles is restricted by the stability prerequisite of the system. The essential gain-boosted telescopic complementary metal–oxide–semiconductor (CMOS) amplifier is given in Fig.5. It has M_1 and M_2 as parts of basic telescopic amplifier. The gain is restricted (around 60 dB for a completely telescopic amplifier) and when the gain is further increased, the parasitic poles turns out to be increasingly predominant and the bandwidth begins to drop. To mitigate this effect additional transistor M_3 is put in a negative feedback loop that makes M_2 less sensitive to the output voltage.

$$g_{m_{2\text{effective}}} = g_{m_2} \left(\frac{g_{m_3}}{g_{d_3}} + 1 \right)$$

- (4) A zero because of the feed-forward way from channel of information transistor to door of the cascade transistor.

The principle goal to change non dominant poles into a couple of complex poles and push the zero past the UGB of the general amplifier and also put an upper limit for division between the complex conjugate poles to optimize the speed. These mentioned enhancements lead to critical gain near limits ($f_T = 1.4$ GHz) for 0.6- μm 3V CMOS process technology.

6. Highly Linear Voltage-Controlled CMOS Transconductors

In this paper 16 circuit strategy for acknowledging voltage-tune able linear high frequency CMOS transconductor cells is portrayed which utilize two cross-coupled MOS transistor sets working in saturation. It utilizes two cross-coupled MOS transistor sets, with one set biased by an extra CMOS voltage source with low output impedance. The system is stretched out to two cross-coupled CMOS transistor sets which gets biasing by a more straightforward voltage source. Two NMOS pairs in the cross-coupled arrangement are so connected that the transistors bulk attached to V_{ss} and V_b , separately, so nobody effects takes place Fig.6.

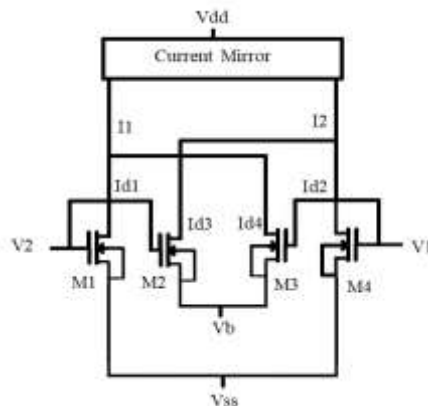


Figure 6. Voltage-Adjustable Cross-Coupled Quad Cell

This circuit arrangement requires a voltage source V_b , with incredibly low output impedance to safeguard the high linearity of the transconductance. A

high-frequency CMOS transconductance component with linearization is obtained from two cross-coupled MOS twofold pairs working in saturation. High frequency cut-off of 370-MHz is obtained through simulated CMOS OTA. A noteworthy element is the wide linear tunability of g_m by a voltage, allowing transconductance values as low as $1\mu S$. The simulation results demonstrate that this system is reasonable good in both low-frequency and high-frequency simple interface circuits for VLSI.

7. Universal Current-Mode OTA-C BIQUAD

In paper¹⁷ present OTA-C biquad, circuit that offers a lot of feature as a realization of low pass, high pass, bandpass, notch, and all pass signals from only single configuration. The circuit made up of two OTAs and two capacitors which are grounded; there are three inputs and four outputs with current mode. In this circuit, the trans conductance are varied through their bias currents. Current transfer functions of the circuit are represented by their equations which are given below

$$(7.1) \quad I_{out} = \frac{\left[s^2 C_1 C_2 I_{in_3} + s C_1 g_2 (I_{in_3} - I_{in_2}) + g_1 g_2 (I_{in_3} - I_{in_1}) \right]}{\Delta}$$

and

$$I_{out_2} = \frac{\left[-s C_2 g_1 I_{in_1} - g_1 g_2 (I_{in_1} - I_{in_2}) \right]}{\Delta}$$

and

$$I_{out_3} = \frac{\left[s C_1 g_2 I_{in_2} + g_1 g_2 I_{in_1} \right]}{\Delta},$$

where $\Delta = s^2 C_1 C_2 + s C_1 g_2 + g_1 g_2$.

By changing the different terms in the numerator in I_{out} different types of filters can be obtained.

(1) High-pass: $I_{in_1} = I_{in_2} = I_{in_3} =$ the input current signal I_{in} .

(2) Band-pass of inverting type: $I_{in_1} = I_{in_3} = 0$ and $I_{in_2} =$ input current signal I_{in} .

(3) Low-pass of inverting type: $I_{in_2} = I_{in_3} = 0$ and $I_{in_1} =$ input current signal I_{in} .

(4) Band-notch: $I_{in1} = 0$ and $I_{in2} = I_{in3} = \text{input current signal } I_{in}$.

(5) All-pass: $I_{in1} = 0$, $I_{in2} = I_{in3}$, and $I_{in3} = \text{input current signal } I_{in}$.

Here all pass filter can obtain from I_{out1} , low pass filter can obtain from output I_{out2} , and band-pass filter from output terminal I_{out3} Fig.7.

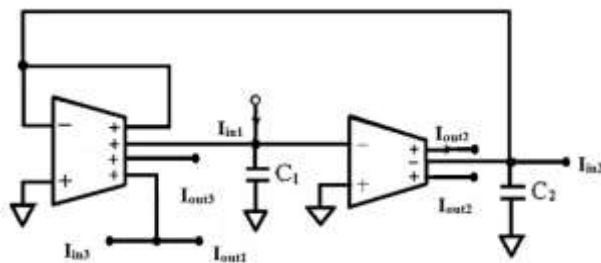


Figure 7. Universal current-mode OTA-C Biquad

Resonance angular frequency (ω_0) and quality factor (Q) of the circuit are represented by two equations, which are given below

$$\omega_0 = \sqrt{\frac{g_1 g_2}{C_1 C_2}} \quad \text{and} \quad \frac{\omega_0}{Q} = \frac{g_2}{C_2}.$$

Filter has low sensitivity because of sensitivities of quality factor and resonance angular frequency is very low. Hand calculated results are verified by simulation results. A lot of work on Bulk Driven, floating gate MOS based Op Amp and OTAs are present that show significant improvement in power performance of circuit by allowing low voltage operation of MOSFET¹⁸. An improved linearity of CMOS based transconductance amplifier is also achievable¹⁹ and active filters designed on CMOS based transconductance amplifier shows improved performance and excellent flexibility²⁰.

8. Conclusion

Four different types of OTA structures are analyzed with operating quality of high DC gain, Speed, Linearity and Design flexibility. The techniques used for low voltage operation is primarily the bulk driven MOS structure. The discussed design architectures can be utilized in Analog CMOS integrated circuits design with specific design objectives. Basic OTA

design structures are also discussed that suggests, there exist a proportionate change of the structures with differential input OTA's and those with single input OTA's. A differential input OTA is identical to two single input OTAs with a similar transconductance g_m however with inverse polarity. Adjusted structures utilizing differential input and differential output OTA's can accomplish exceptionally high common-mode rejection ratio (CMRR) and lessen both the even-order harmonic distortion segments and the impacts of the power supply noise. This paper has covered a review of papers addressing major issues of high frequency gain, high linearity, low energy and design flexibility of OTAs which can be helpful in designing analog integrated circuit for different applications.

References

1. Ko-Chi Kuo and A. Leuciuc, A Linear MOS Transconductor using Source Degeneration and Adaptive Biasing, *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, **48(10)** (2001), 937-943.
2. S. Szczepanski, R. Schaumann and P. Wu, Linear Transconductor Based on Crosscoupled CMOS Pairs, *Electronics Letters*, **27(9)** (1991), 783-785.
3. T. Deliyannis, Y. Sun and J.K. Fidler, *Continuous-time active filter design*, CRC Press, 2019.
4. R. L. Geiger and E. Sánchez-Sinencio, Active Filter Design using Operational Transconductance Amplifiers: A Tutorial, *IEEE Circuits and Devices Magazine*, **1(2)** (1985), 20-32.
5. G. Meyer-Brotz and A. Kley, The Common-Mode Rejection of Transistor Differential Amplifiers, *IEEE Transactions on Circuit Theory*, **13(2)** (1966), 171-175.
6. A. N. Mohieldin, E. Sanchez-Sinencio and J. Silva-Martinez, A Fully Balanced Pseudo-Differential OTA with Common-Mode Feedforward and Inherent Common-Mode Feedback Detector, *IEEE Journal of Solid-State Circuits*, **38(4)** (2003), 63-668.
7. T. Y. Wang, L. H. Liu and S.Y. Peng, A Power-Efficient Highly Linear Reconfigurable Biopotential Sensing Amplifier using Gate-Balanced Pseudoresistors, *IEEE Transactions on Circuits and Systems II: Express Briefs*, **62(2)** (2015), 199-203.
8. T. Kulej, 0.5-V Bulk-Driven CMOS Operational Amplifier, *IET Circuits, Devices & Systems*, **7(6)** (2013), 352-360.
9. F. Khateband S. Vlassis, Low-Voltage Bulk-Driven Rectifier for Biomedical Applications, *Microelectronics Journal*, **44(8)** (2013), 642-648.
10. F. Khateb, M. Kumngern, V. Spyridon and C. Psychalinos, Differential Difference Current Conveyor using Bulk-Driven Technique for Ultra-Low-Voltage Applications, *Circuits, Systems, and Signal Processing*, **33(1)** (2014), 159-176.

11. A. I. A. Cunha, M. C. Schneider and C. Galup-Montoro, An MOS Transistor Model for Analog Circuit Design, *IEEE Journal of Solid-State Circuits*, **33(10)** (1998), 1510-1519.
12. S. S. Hassani and A. Golmakani, A 0.5 V, 900uW CMOS OTA using Bulk Driven and Hybrid Compensation Technique, *Majlesi Journal of Telecommunication Devices*, **3(2)** (2014).
13. X. Zhao, H. Fang, T. Ling and J. Xu, Transconductance Improvement Method for Low-Voltage Bulk-Driven Input Stage, *Integration*, **49** (2015), 98-103.
14. J. Rosenfeld, M. Kozak and E. G. Friedman, A Bulk-Driven CMOS OTA with 68 Db DC Gain, *Proceedings of the 2004 11th IEEE International Conference on Electronics, Circuits and Systems*, (2004), 5-8.
15. M. Das, Improved Design Criteria of Gain-Boosted CMOS OTA with High-Speed Optimizations, *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, **49(3)** (2002), 204-207.
16. S. Szczepanski, A. Wyszynski and R. Schaumann, Highly Linear Voltage-Controlled CMOS Transconductors, *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, **40(4)** (1993), 258-262.
17. C. M. Chang and S. K. Pai, Universal Current-Mode OTA-C Biquad with the Minimum Components, *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, **47(8)** (2000), 1235-1238.
18. L. Zuo and S. K. Islam, Low-Voltage Bulk-Driven Operational Amplifier with Improved Transconductance, *IEEE Transactions on Circuits and Systems I: Regular Papers*, **60(8)** (2013), 2084-2091.
19. S. Szczepanski, A. Wyszynski and R. Schaumann, Highly Linear Voltage-Controlled CMOS Transconductors, *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, **40(4)** (1993), 258-262.
20. E. Sánchez-Sinencio and J. Silva-Martínez, CMOS Transconductance Amplifiers, Architectures and Active Filters: A Tutorial, *IEEE Proceedings-Circuits, Devices and Systems*, **147(1)** (2000), 3-12.